R13

Code No: 126EN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year II Semester Examinations, May - 2016
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define g_m of MOS transistor. [2]
b) Draw transfer characteristics of CMOS inverter. [3]
c) Define scaling and explain it. [2]
d) Explain difference between stick diagram and layout diagram. [3]
e) Define delay and explain different time delays in gate level modeling. [2]
f) Explain the importance of wiring capacitance of a MOS transistor. [3]
g) Explain the difference between EPROM and EEPROM. [2]
h) Draw 2-bit comparator. [3]
i) Explain difference between PLA and PAL. [2]
j) Define controllability and observability with respect to testing. [3]

PART - B

(50 Marks)

2. Draw the fabrication steps of CMOS transistor and explain its operation in detail. [10]

OR

3. Draw the fabrication steps of NMOS transistor and explain its operation in detail. [10]

4.a) Draw the flow chart of VLSI Design flow and explain the operation of each step in detail.
b) Draw the stick diagram for three input AND gate. [6+4]

OR

5. What is the purpose of design rule? What is the purpose of stick diagram? What are the different approaches for describing the design rule? Give three approaches for making contacts between poly silicon and discussion in NMOS circuit. [10]

6.a) Draw and explain fan in and fan out characteristics of different CMOS design technologies.
b) Explain different wiring capacitance used in Gate level design with example. [5+5]

OR

7. What are the alternate gate circuits available? Explain any one of item with suitable sketch by taking NAND gate as an example. [10]

Draw the basic circuit diagram of static RAM and explain its operation.
Draw the basic block diagram of 4-bit adder and explain its operation in detail. [5+5]

OR

a) Explain the CMOS system design based on the I/O cells with suitable example.
b) Design a four bit parity generator using only XOR gates and draw the Schematic of it. [5+5]

10.a) Why the chip testing is needed? At what levels testing a chip can occur?
b) What is the drawback of serial scan? How to overcome this? [5+5]

OR

11.a) Briefly Explain different parameters influencing low power design in detail.
b) What is sequential fault grading? Explain how it is analyzed. [5+5]

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