R09

Code No: 58033

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, May - 2016
DIGITAL DESIGN THROUGH VERILOG HDL
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

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1.a) Define simulation and explain different simulation techniques used in HDL.
b) Explain the term concurrency and give the different concurrency statements used in HDL. [8+7]

2.a) Explain the different operators used in Verilog HDL with examples.
b) Explain the importance of Data types used in verilog and give the different data types for it. [8+7]

3.a) Write a Verilog HDL code for JK flip-flop along with gate primitives and draw its timing diagram for it.
b) Explain the concept of different Delays used in Gate level modeling. [8+7]

4. Explain the blocking and non-blocking assignments statements used in Behavioral modeling along with examples. [15]

5.a) Explain the importance of switch level modeling in verilog HDL.
b) Draw the CMOS inverter circuit diagram and explain its operation in detail. [8+7]

6.a) Give the different system tasks and functions used in Verilog HDL with examples.
b) Explain the concept of different user defined primitives with examples. [8+7]

7. Explain the following terms in detail with examples.
a) Capacitive model b) feedback model. [8+7]

8. Draw the Combinational circuit testing with example and explain the test bench verification for it. [15]

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