Code No: 07A30401　　　　　R07　　　　Set No. 2

II B.Tech I Semester Examinations,November 2010
PULSE AND DIGITAL CIRCUITS
Common to Electronics And Instrumentation Engineering, Electrical And
Electronics Engineering

Time: 3 hours　　　　　　　　　　　　　　　　　　Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Define the following:
   i. Storage time
   ii. Delay time
   iii. Rise time
   iv. Fall time

   (b) Explain how a BJT can be used as a switch. Compare its perfoemance as a switch with JFET. [8+8]

2. (a) Describe frequency division employing a transistor astable multivibrator with waveforms.

   (b) Describe frequency division employing a transistor monostable multivibrator with waveforms. [8+8]

3. (a) What is pedestal? Illustrate the effect of control voltage on gate output.

   (b) Write the advantages and disadvantages of unidirectional diode gate. [16]

4. (a) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation.

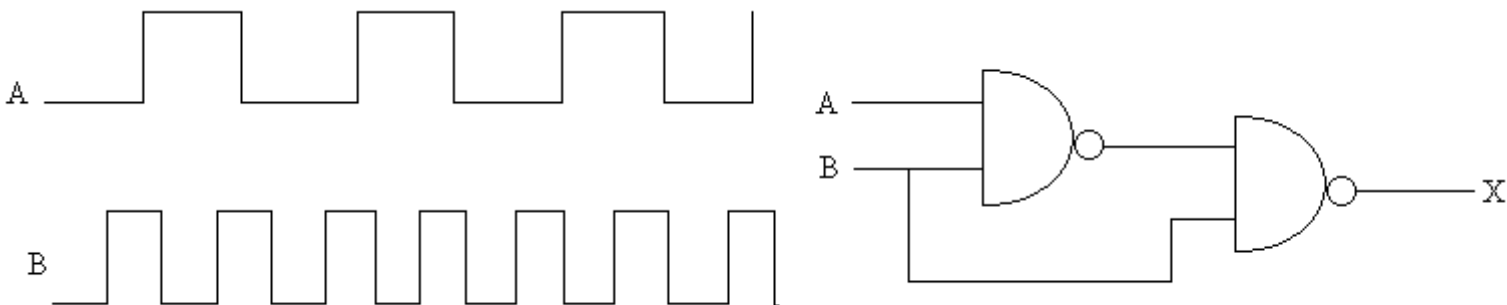   (b) Draw the output waveform X for the given inputs figure 3b

Figure 3b

5. Consider a self-biased nonsaturated flip-flop obtained from figure 2 by setting V_{BB}=0 and by adding a common emitter resistor Re to ground in figure 2. The circuit has the following parameters:　　V_{CC}=25V,V_Z=4.3V, h_{FE}= 50, Rc=2.2K,R_1=R_2=15K and Re=470Ω. Neglect the voltage drop across a forward-biased junction. Verify that the transistors do not enter the saturation region. Calculate the transistor

currents and the current in each diode.   [16]
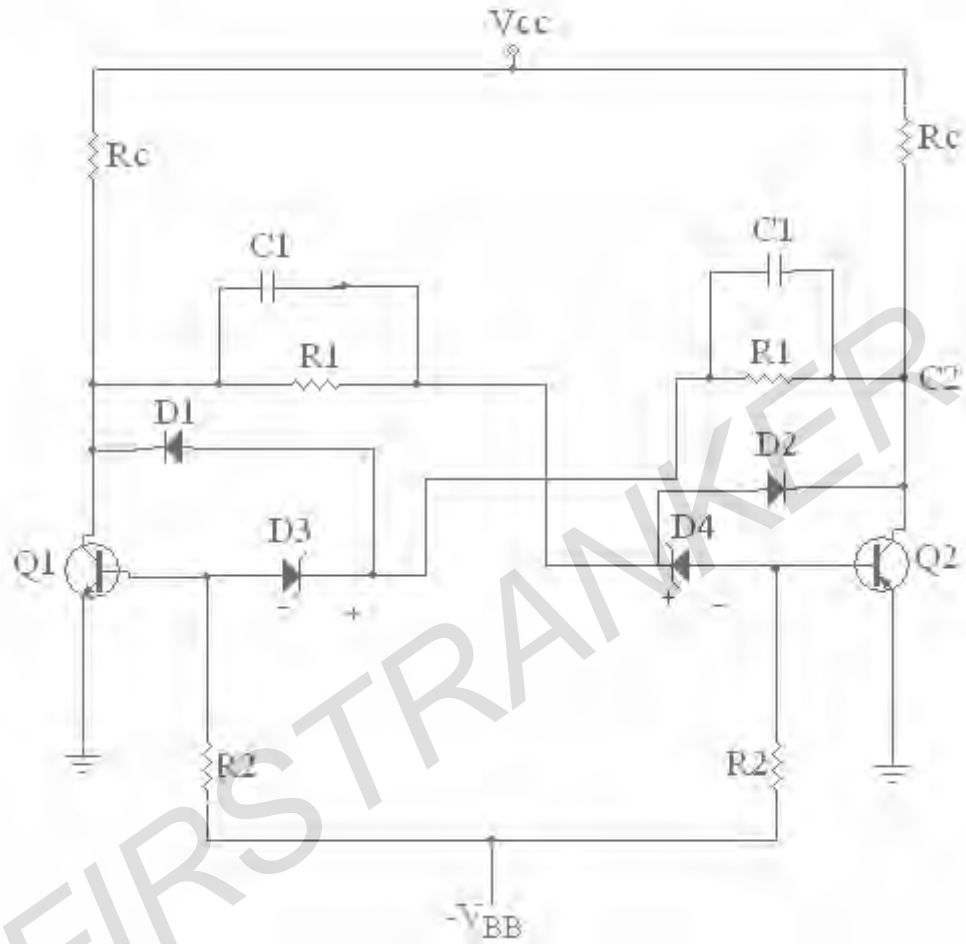

Figure 2

6. (a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the figure 4a.
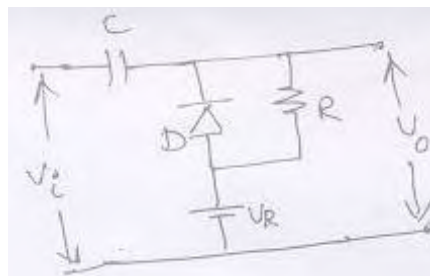

Figure 4a

   (b) Compare series diode clipper and shunt diode clipper.   [8+8]

7. (a) List out the applications of sweep circuits.

   (b) Distinguish between voltage and current sweep circuits.

   (c) Draw the circuit of a linear current sweep and explain its operation with wave-forms. Explain the necessity of generating trapezoidal waveform.   [4+4+8]

2

8. (a) Obtain the response of RC high pass cirucit for an exponential i/p lignal

   (b) A square wave whose peak-to-peak valve is 1 V, exterds $\pm$ 0.5V w.r.t. to ground. The half period is 0.1 Sec this voltage impressed upon an RC differentating circuit whose time constant is 0.2 sec. Determine the maximum and minimum values of the o/p voltages in the steady state.   [8+8]

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3

Code No: 07A30401 **R07** **Set No. 4**

II B.Tech I Semester Examinations,November 2010
PULSE AND DIGITAL CIRCUITS
Common to Electronics And Instrumentation Engineering, Electrical And
Electronics Engineering

Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation.

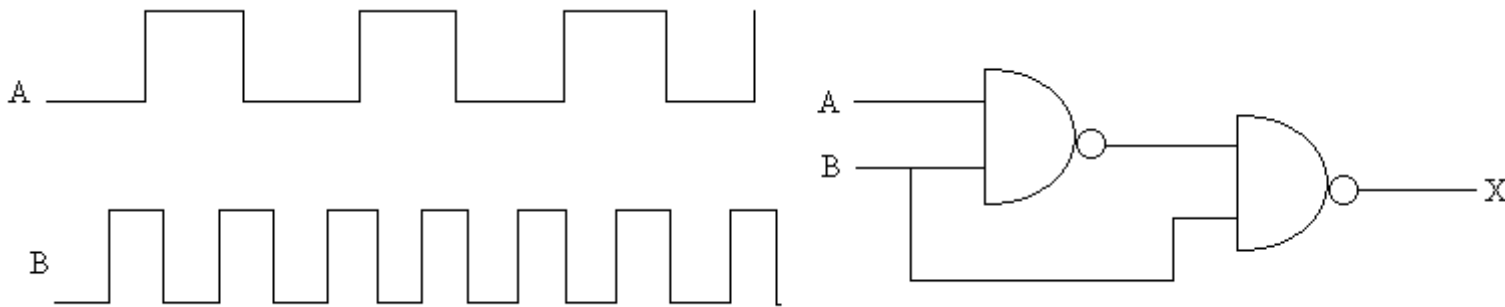   (b) Draw the output waveform X for the given inputs figure 3b

Figure 3b

2. (a) What is pedestal? Illustrate the effect of control voltage on gate output.

   (b) Write the advantages and disadvantages of unidirectional diode gate.   [16]

3. (a) Describe frequency division employing a transistor astable multivibrator with waveforms.

   (b) Describe frequency division employing a transistor monostable multivibrator with waveforms.   [8+8]

4. (a) Define the following:

       i. Storage time
       ii. Delay time
       iii. Rise time
       iv. Fall time

   (b) Explain how a BJT can be used as a switch. Compare its perfoemance as a switch with JFET.   [8+8]

5. (a) Obtain the response of RC high pass cirucit for an exponential i/p lignal

   (b) A square wave whose peak-to-peak valve is 1 V, exterds ± 0.5V w.r.t. to ground. The half period is 0.1 Sec this voltage impressed upon an RC differentating circuit whose time constant is 0.2 sec. Determine the maximum and minimum values of the o/p voltages in the steady state.   [8+8]

4

6. Consider a self-biased nonsaturated flip-flop obtained from figure 2 by setting $V_{BB}=0$ and by adding a common emitter resistor Re to ground in figure 2. The circuit has the following parameters: $V_{CC}=25V, V_Z=4.3V, h_{FE}=50, Rc=2.2K, R_1=R_2=15K$ and $Re=470\Omega$. Neglect the voltage drop across a forward-biased junction. Verify that the transistors do not enter the saturation region. Calculate the transistor currents and the current in each diode. [16]
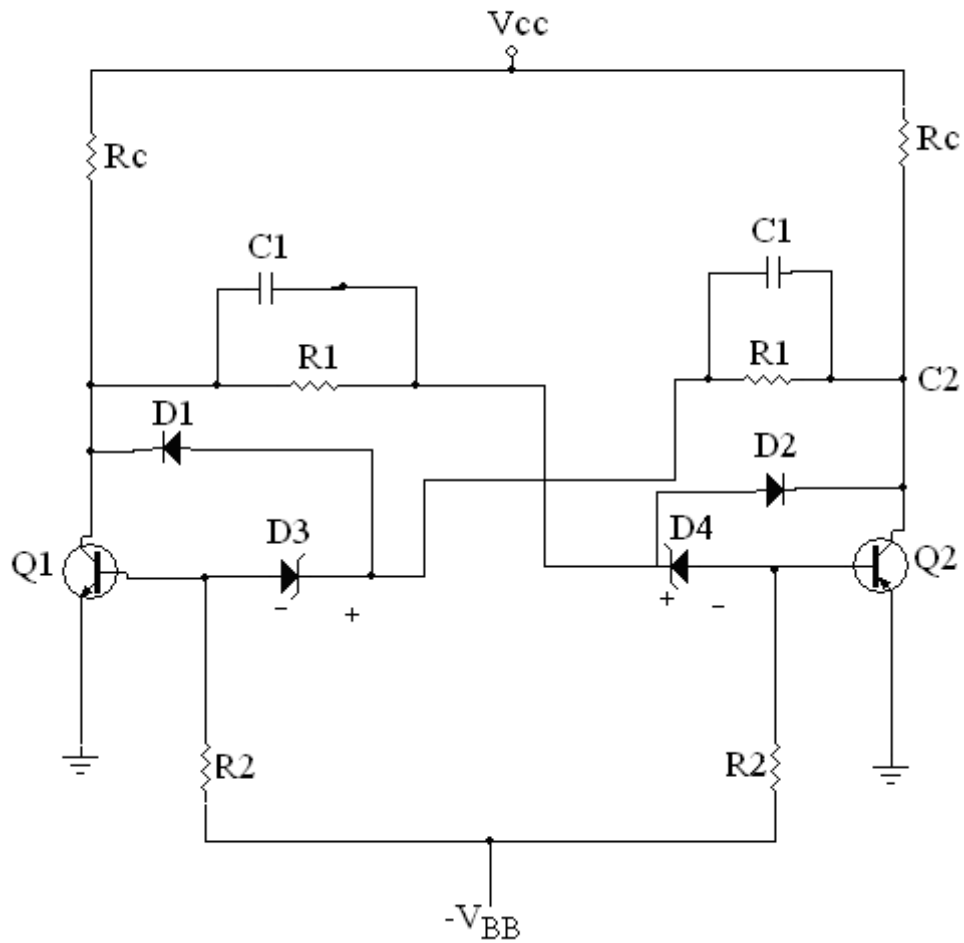

Figure 2

7. (a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the figure 4a.
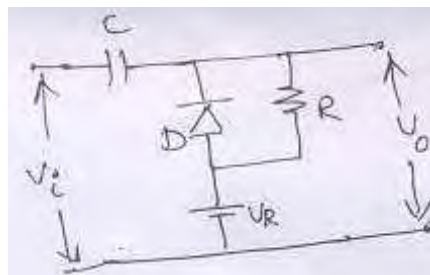

Figure 4a

(b) Compare series diode clipper and shunt diode clipper. [8+8]

R07

Set No. 4

8. (a) List out the applications of sweep circuits.

   (b) Distinguish between voltage and current sweep circuits.

   (c) Draw the circuit of a linear current sweep and explain its operation with waveforms. Explain the necessity of generating trapezoidal waveform.   [4+4+8]

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FIRSTRANKER

R07

Set No. 1

II B.Tech I Semester Examinations,November 2010
PULSE AND DIGITAL CIRCUITS
Common to Electronics And Instrumentation Engineering, Electrical And
Electronics Engineering

Time: 3 hours   Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks
$\star\star\star\star\star$

1. (a) Obtain the response of RC high pass cirucit for an exponential i/p lignal

   (b) A square wave whose peak-to-peak valve is 1 V, exterds $\pm$ 0.5V w.r.t. to ground. The half period is 0.1 Sec this voltage impressed upon an RC differentating circuit whose time constant is 0.2 sec. Determine the maximum and minimum values of the o/p voltages in the steady state. [8+8]

2. (a) What is pedestal? Illustrate the effect of control voltage on gate output.

   (b) Write the advantages and disadvantages of unidirectional diode gate. [16]

3. (a) Describe frequency division employing a transistor astable multivibrator with waveforms.

   (b) Describe frequency division employing a transistor monostable multivibrator with waveforms. [8+8]

4. (a) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation.

   (b) Draw the output waveform X for the given inputs figure 3b
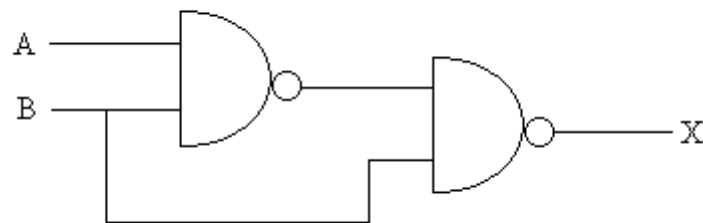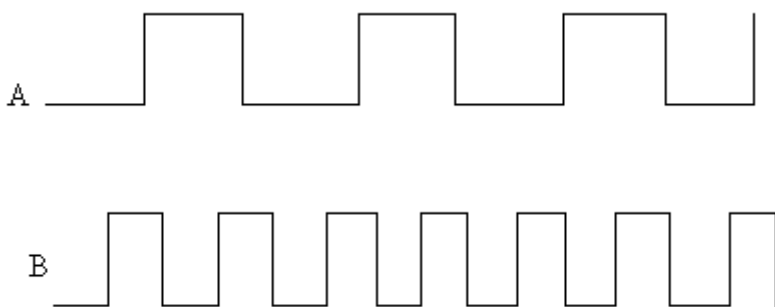

Figure 3b

5. (a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the figure 4a.
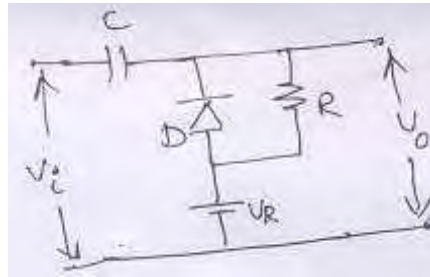
Figure 4a

(b) Compare series diode clipper and shunt diode clipper. [8+8]

6. (a) List out the applications of sweep circuits.

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    ii. Delay time

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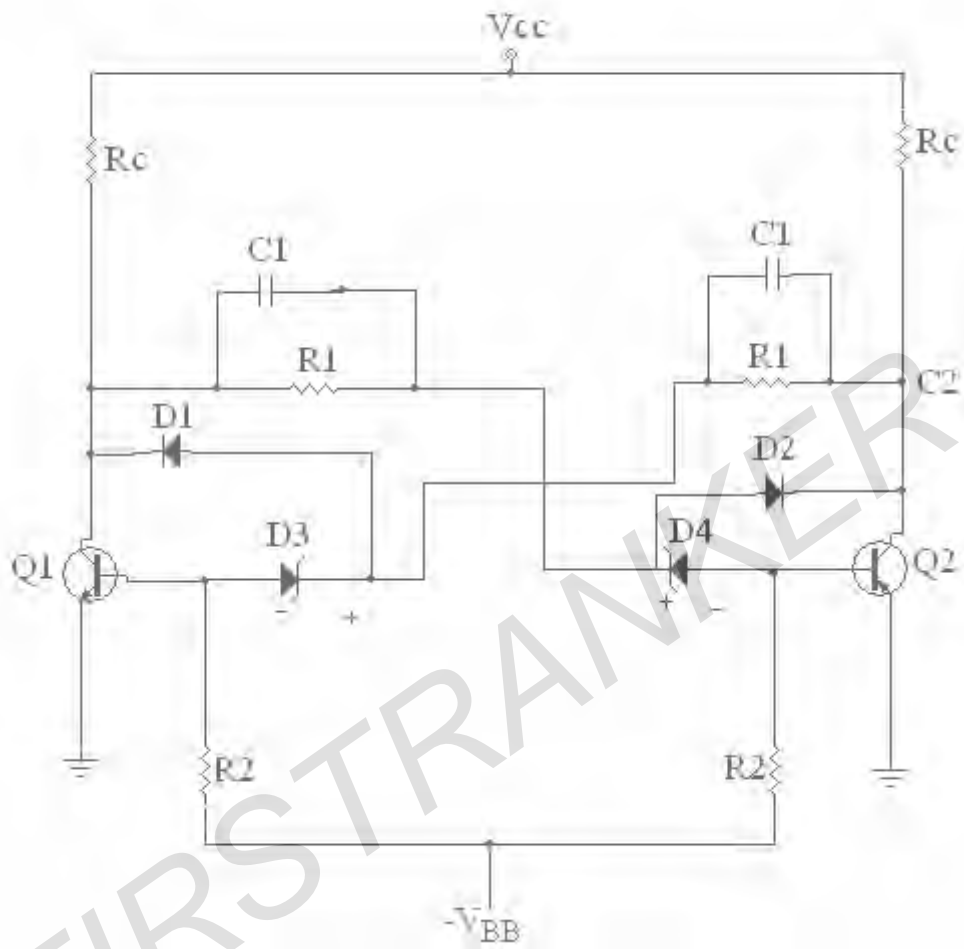
Figure 2

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Code No: 07A30401 **R07** **Set No. 3**

II B.Tech I Semester Examinations,November 2010
PULSE AND DIGITAL CIRCUITS
Common to Electronics And Instrumentation Engineering, Electrical And
Electronics Engineering
Time: 3 hours   Max Marks: 80
Answer any FIVE Questions
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⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Obtain the response of RC high pass cirucit for an exponential i/p lignal

    (b) A square wave whose peak-to-peak valve is 1 V, exterds ± 0.5V w.r.t. to
    ground. The half period is 0.1 Sec this voltage impressed upon an RC dif-
    ferentating circuit whose time constant is 0.2 sec. Determine the maximum
    and minimum values of the o/p voltages in the steady state.   [8+8]

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   V_{BB}=0 and by adding a common emitter resistor Re to ground in figure 2. The cir-
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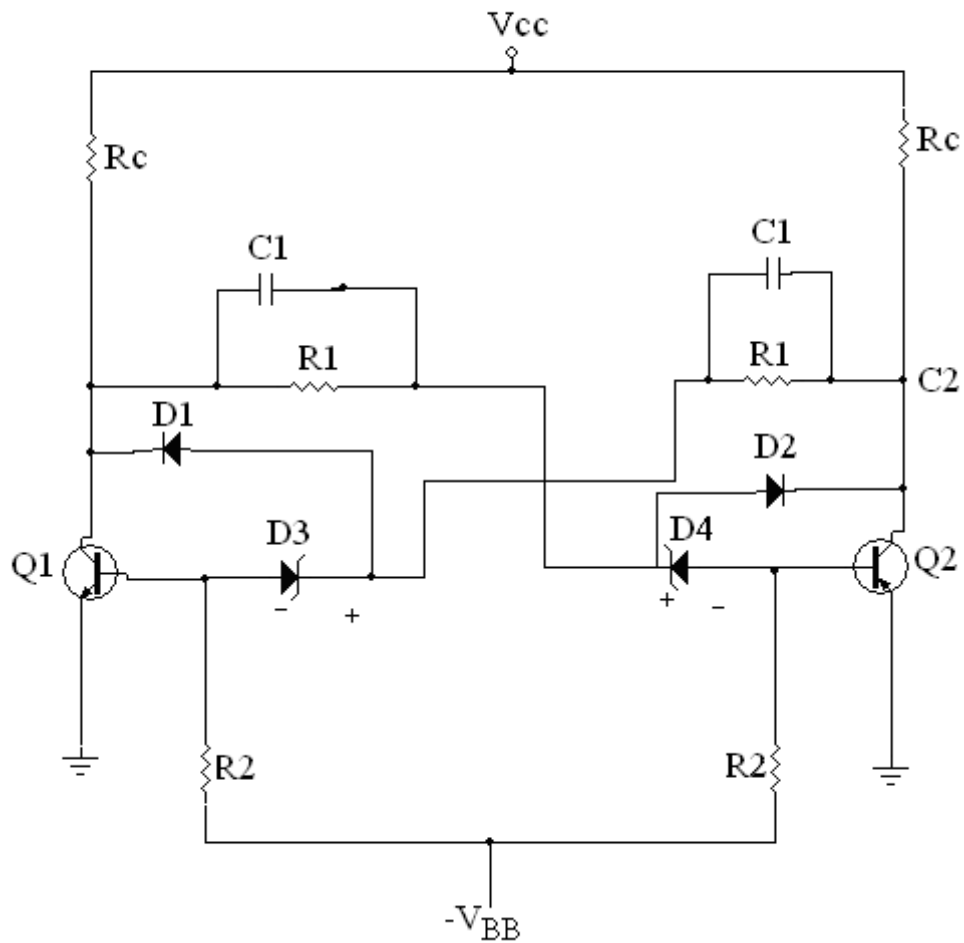
Figure 2

3. (a) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation.

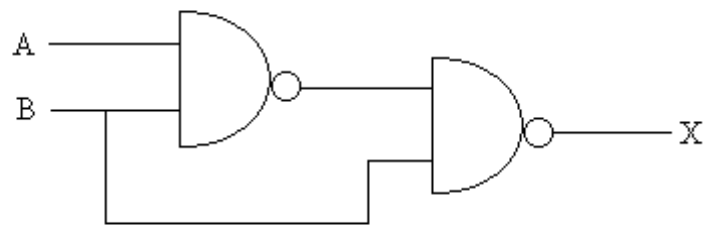(b) Draw the output waveform X for the given inputs figure 3b
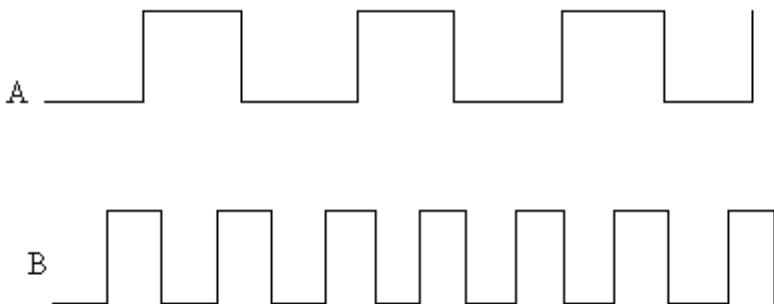

Figure 3b

4. (a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the figure 4a.

Figure 4a

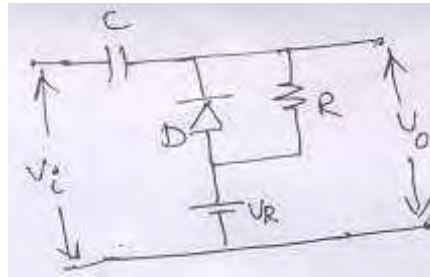(b) Compare series diode clipper and shunt diode clipper. [8+8]

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