Code No: 07A3EC03 **R07** **Set No. 2**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit diagram of a 4-bit subtractor, adder using 2's complement method
   (b) Design a logic circuit to encode a 2^n input bits to n bit output. [8+8]

2. (a) Given the binary numbers A = 1110.1, B = 100.01, C = 10011.1 Perform the following binary operations:
      i. A+B
      ii. AB
      iii. A. B
      iv. A / B
   (b) Explain the procedure to convert a hexadecimal number to a decimal number with an example. [12+4]

3. Discuss about Threshold logic. Explain the Capabilities and limitations of Threshold gate. [16]

4. A State table is given below. It is the minimal state table. Give a proper state assignment. Design the circuit for this state table using JK flip flop. [16]

PS	NEXT STATE		Out put, Z	
	X = 0	X = 1	X = 0	X = 1
A	B	A	1	1
B	C	A	1	0
C	D	E	0	0
D	D	A	0	1
E	B	A	1	1

5. (a) State the purpose of reducing the switching functions to minimal form
   (b) Write the Dual of
      i. (A+BC′+AB)
      ii. (AB+B′C+CD)
   (c) Give the truth table for the Boolean expression (X′+Y)′ [4+8+4]

6. Using Q-M method to determine the prime implicants and obtain the possible minimal expression for the following function
   F(A,B,C,D) = Σm(8,12,13,18,19,21,22,24,25,28,30,31) + d(1,2,4,6,7,11,26) [16]

7. A sequential circuit has 2 flip flops (A and B), two inputs (x and y), and an output (z). The state equations are given as
   JA = xB + $y'B'$ KA = $xy'B'$
   JB = xA$'$ KB = xy$'$ + A
   Z = xyA + $x'y'B$
   Obtain the state table and state diagram from the state equations. Draw an ASM chart for the above mentioned design. [16]

8. (a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.
   (b) Design a basic flip flop and explain its operation. [8+8]

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Code No: 07A3EC03 **R07** **Set No. 4**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Using Q-M method to determine the prime implicants and obtain the possible minimal expression for the following function
F(A,B,C,D) = Σm(8,12,13,18,19,21,22,24,25,28,30,31) + d(1,2,4,6,7,11,26) [16]

2. A sequential circuit has 2 flip flops (A and B), two inputs (x and y), and an output (z). The state equations are given as
JA = xB + $y'B'$ KA = $xy'B'$
JB = xA′ KB = xy′ + A
Z = xyA + $x'y'B$
Obtain the state table and state diagram from the state equations. Draw an ASM chart for the above mentioned design. [16]

3. (a) Draw the circuit diagram of a 4-bit subtractor, adder using 2's complement method
   (b) Design a logic circuit to encode a 2^n input bits to n bit output. [8+8]

4. (a) State the purpose of reducing the switching functions to minimal form
   (b) Write the Dual of
      i. (A+BC′+AB)
      ii. (AB+B′C+CD)
   (c) Give the truth table for the Boolean expression (X′+Y)′ [4+8+4]

5. (a) Given the binary numbers A = 1110.1, B = 100.01, C = 10011.1 Perform the following binary operations:
      i. A+B
      ii. AB
      iii. A. B
      iv. A / B
   (b) Explain the procedure to convert a hexadecimal number to a decimal number with an example. [12+4]

6. (a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.
   (b) Design a basic flip flop and explain its operation. [8+8]

7. A State table is given below. It is the minimal state table. Give a proper state assignment. Design the circuit for this state table using JK flip flop. [16]

PS	NEXT STATE		Out put, Z	
	X = 0	X = 1	X = 0	X = 1
A	B	A	1	1
B	C	A	1	0
C	D	E	0	0
D	D	A	0	1
E	B	A	1	1

8. Discuss about Threshold logic. Explain the Capabilities and limitations of Threshold gate. [16]

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Code No: 07A3EC03 **R07** **Set No. 1**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

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1. A State table is given below. It is the minimal state table. Give a proper state assignment. Design the circuit for this state table using JK flip flop. [16]

PS	NEXT STATE		Out put, Z	
	X = 0	X = 1	X = 0	X = 1
A	B	A	1	1
B	C	A	1	0
C	D	E	0	0
D	D	A	0	1
E	B	A	1	1

2. (a) Draw the circuit diagram of a 4-bit subtractor, adder using 2's complement method
   (b) Design a logic circuit to encode a 2^n input bits to n bit output. [8+8]

3. A sequential circuit has 2 flip flops (A and B), two inputs (x and y), and an output (z). The state equations are given as
   JA = xB + $y'B'$ KA = $xy'B'$
   JB = xA′ KB = xy′ + A
   Z = xyA + $x'y'B$
   Obtain the state table and state diagram from the state equations. Draw an ASM chart for the above mentioned design. [16]

4. (a) Given the binary numbers A = 1110.1, B = 100.01, C = 10011.1 Perform the following binary operations:
      i. A+B
      ii. AB
      iii. A. B
      iv. A / B
   (b) Explain the procedure to convert a hexadecimal number to a decimal number with an example. [12+4]

5. (a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.
   (b) Design a basic flip flop and explain its operation. [8+8]

6. Using Q-M method to determine the prime implicants and obtain the possible minimal expression for the following function
   F(A,B,C,D) = Σm(8,12,13,18,19,21,22,24,25,28,30,31) + d(1,2,4,6,7,11,26) [16]

7. Discuss about Threshold logic. Explain the Capabilities and limitations of Threshold gate. [16]

8. (a) State the purpose of reducing the switching functions to minimal form
   (b) Write the Dual of
      i. (A+BC′+AB)
      ii. (AB+B′C+CD)
   (c) Give the truth table for the Boolean expression (X′+Y)′ [4+8+4]

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Code No: 07A3EC03 **R07** **Set No. 3**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Using Q-M method to determine the prime implicants and obtain the possible minimal expression for the following function
$F(A,B,C,D) = \Sigma m(8,12,13,18,19,21,22,24,25,28,30,31) + d(1,2,4,6,7,11,26)$ [16]

2. (a) State the purpose of reducing the switching functions to minimal form
   (b) Write the Dual of
      i. $(A+BC'+AB)$
      ii. $(AB+B'C+CD)$
   (c) Give the truth table for the Boolean expression $(X'+Y)'$ [4+8+4]

3. (a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.
   (b) Design a basic flip flop and explain its operation. [8+8]

4. (a) Given the binary numbers A = 1110.1, B = 100.01, C = 10011.1 Perform the following binary operations:
      i. A+B
      ii. AB
      iii. A. B
      iv. A / B
   (b) Explain the procedure to convert a hexadecimal number to a decimal number with an example. [12+4]

5. A State table is given below. It is the minimal state table. Give a proper state assignment. Design the circuit for this state table using JK flip flop. [16]

PS	NEXT STATE		Out put, Z	
	X = 0	X = 1	X = 0	X = 1
A	B	A	1	1
B	C	A	1	0
C	D	E	0	0
D	D	A	0	1
E	B	A	1	1

6. Discuss about Threshold logic. Explain the Capabilities and limitations of Threshold gate. [16]

7. (a) Draw the circuit diagram of a 4-bit subtractor, adder using 2's complement method

   (b) Design a logic circuit to encode a 2^n input bits to n bit output. [8+8]

8. A sequential circuit has 2 flip flops (A and B), two inputs (x and y), and an output (z). The state equations are given as
   JA = xB + $y'B'$ KA = $xy'B'$
   JB = xA$'$ KB = xy$'$ + A
   Z = xyA + $x'y'B$
   Obtain the state table and state diagram from the state equations. Draw an ASM chart for the above mentioned design. [16]

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