Code No: 07A3EC14 **R07** **Set No. 2**

II B.Tech I Semester Examinations,November 2010
ELECTRONIC CIRCUIT ANALYSIS
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) For a single stage transistor amplifier, R_S = 10K and R_L= 10K. The h-parameter values are $h_{fc} = -51$, h_{ic} =1.1KΩ, $h_{rc} \approx 1, h_{oc}$ = 25 μA/V Find A_I, A_V, A_{VS}, R_i, and R_o for the CC transistor configuration.

   (b) For a single stage transistor amplifier, R_S=1KΩ, and R_L= 10K The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10^{-4}, h_{oe} = 25 μ A/V. Find A_I, A_V, A_{VS}, R_i, and R_o for the CE transistor configuration. [8+8]

2. (a) Define the terms:

      i. Load Regulation
      ii. Line Regulation
      iii. Ripple Rejection
      iv. Sense Voltage

   (b) In a zener diode regulator,
   Vi_{nom} = 40V,Vi_{min} = 35V, Vi_{max} = 45V V_z = 20V, r_z = 5 ohms I_{Lmin}= 0mA,I_{Lmax} = 100mA I_{zmin} = 10mA, I_{zmax} = 400mA. Find P_{zmax} and load resistance. [8+8]

3. (a) The basic Switching regulator is designed to maintain a 12V dc output when the unregulated input voltage varies from 15V to 24V. When pass transistor is conducting, its collector to emitter saturation voltage is 0.5V. Assuming that the load is constant and the LC filter is ideal, find the minimum and maximum duty cycles of the pulse width modulator.

   (b) Write the Features and Applications of DC/DC converters [8+8]

4. (a) Derive the expression for the high 3-dB frequency f_h^* of n-identical non interacting stages in terms of f_H for one stage.

   (b) If four identical amplifiers are cascaded each having f_H =100 KHz, determine the overall upper 3dB frequency f_h^*. Assume non interacting stages.

   (c) Write a short note on Bootstrapped Darlington circuit. [5+5+6]

5. Draw the circuit diagram of a class-B tuned amplifier. Explain its operation with neat waveforms. Also derive the expression for percentage efficiency and maximum power dissipation. [16]

6. Draw the circuit diagram of a Double tuned amplifier and derive the expression for 3-dB bandwidth. [16]

7. (a) Show that in Hybrid - π model, the diffusion capacitance is proportional to the emitter bias current.

   (b) What is the frequency range to consider Giacolletto model of a transistor at high frequencies? What is the significance of f_T in discussing the frequency range of a transistor at high frequencies? [8+8]

8. (a) Draw the circuit of class -A series fed power amplifier and derive the expression for output power P_o. [10]

   (b) Draw and discuss the operation of Class - C power amplifier. [6]

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Code No: 07A3EC14 **R07** **Set No. 4**

II B.Tech I Semester Examinations,November 2010
ELECTRONIC CIRCUIT ANALYSIS
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Draw the circuit diagram of a Double tuned amplifier and derive the expression for 3-dB bandwidth. [16]

2. (a) Define the terms:
   i. Load Regulation
   ii. Line Regulation
   iii. Ripple Rejection
   iv. Sense Voltage

   (b) In a zener diode regulator,
   $Vi_{nom} = 40V$, $Vi_{min} = 35V$, $Vi_{max} = 45V$ $V_z = 20V$, $r_z = 5$ ohms $I_{Lmin} = 0mA$, $I_{Lmax} = 100mA$ $I_{zmin} = 10mA$, $I_{zmax} = 400mA$. Find P_{zmax} and load resistance. [8+8]

3. (a) The basic Switching regulator is designed to maintain a 12V dc output when the unregulated input voltage varies from 15V to 24V. When pass transistor is conducting, its collector to emitter saturation voltage is 0.5V. Assuming that the load is constant and the LC filter is ideal, find the minimum and maximum duty cycles of the pulse width modulator.

   (b) Write the Features and Applications of DC/DC converters [8+8]

4. (a) Draw the circuit of class -A series fed power amplifier and derive the expression for output power P_o. [10]

   (b) Draw and discuss the operation of Class - C power amplifier. [6]

5. (a) Show that in Hybrid - π model, the diffusion capacitance is proportional to the emitter bias current.

   (b) What is the frequency range to consider Giacolletto model of a transistor at high frequencies? What is the significance of f_T in discussing the frequency range of a transistor at high frequencies? [8+8]

6. Draw the circuit diagram of a class-B tuned amplifier. Explain its operation with neat waveforms. Also derive the expression for percentage efficiency and maximum power dissipation. [16]

7. (a) Derive the expression for the high 3-dB frequency f_h^* of n-identical non interacting stages in terms of f_H for one stage.

(b) If four identical amplifiers are cascaded each having f_H =100 KHz, determine the overall upper 3dB frequency f_h^*. Assume non interacting stages.

(c) Write a short note on Bootstrapped Darlington circuit. [5+5+6]

8. (a) For a single stage transistor amplifier, R_S = 10K and R_L= 10K. The h-parameter values are $h_{fc} = -51$, h_{ic} =1.1KΩ, $h_{rc} \approx 1, h_{oc} = 25$ μA/V Find A_I, A_V, A_{VS}, R_i, and R_o for the CC transistor configuration.

(b) For a single stage transistor amplifier, R_S=1KΩ, and R_L= 10K The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10^{-4}, h_{oe} = 25 μ A/V. Find A_I, A_V, A_{VS}, R_i, and R_o for the CE transistor configuration. [8+8]

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Code No: 07A3EC14 **R07** **Set No. 1**

II B.Tech I Semester Examinations,November 2010
ELECTRONIC CIRCUIT ANALYSIS
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) The basic Switching regulator is designed to maintain a 12V dc output when the unregulated input voltage varies from 15V to 24V. When pass transistor is conducting, its collector to emitter saturation voltage is 0.5V. Assuming that the load is constant and the LC filter is ideal, find the minimum and maximum duty cycles of the pulse width modulator.

   (b) Write the Features and Applications of DC/DC converters [8+8]

2. Draw the circuit diagram of a class-B tuned amplifier. Explain its operation with neat waveforms. Also derive the expression for percentage efficiency and maximum power dissipation. [16]

3. (a) Derive the expression for the high 3-dB frequency f_h^* of n-identical non interacting stages in terms of f_H for one stage.

   (b) If four identical amplifiers are cascaded each having f_H =100 KHz, determine the overall upper 3dB frequency f_h^*. Assume non interacting stages.

   (c) Write a short note on Bootstrapped Darlington circuit. [5+5+6]

4. (a) For a single stage transistor amplifier, R_S = 10K and R_L= 10K. The h-parameter values are $h_{fc} = -51$, h_{ic} =1.1KΩ, $h_{rc} \approx 1, h_{oc} = 25$ μA/V Find A_I, A_V, A_{VS}, R_i, and R_o for the CC transistor configuration.

   (b) For a single stage transistor amplifier, R_S=1KΩ, and R_L= 10K The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10^{-4}, h_{oe} = 25 μ A/V. Find A_I, A_V, A_{VS}, R_i, and R_o for the CE transistor configuration. [8+8]

5. (a) Define the terms:
      i. Load Regulation
      ii. Line Regulation
      iii. Ripple Rejection
      iv. Sense Voltage

   (b) In a zener diode regulator,
   Vi_{nom} = 40V,Vi_{min} = 35V, Vi_{max} = 45V V_z = 20V, r_z = 5 ohms I_{Lmin}= 0mA,I_{Lmax} = 100mA I_{zmin} = 10mA, I_{zmax} = 400mA. Find P_{zmax} and load resistance. [8+8]

6. Draw the circuit diagram of a Double tuned amplifier and derive the expression for 3-dB bandwidth. [16]

7. (a) Show that in Hybrid - π model, the diffusion capacitance is proportional to the emitter bias current.

   (b) What is the frequency range to consider Giacolletto model of a transistor at high frequencies? What is the significance of f_T in discussing the frequency range of a transistor at high frequencies? [8+8]

8. (a) Draw the circuit of class -A series fed power amplifier and derive the expression for output power P_o. [10]

   (b) Draw and discuss the operation of Class - C power amplifier. [6]

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Code No: 07A3EC14 **R07** **Set No. 3**

II B.Tech I Semester Examinations,November 2010
ELECTRONIC CIRCUIT ANALYSIS
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) The basic Switching regulator is designed to maintain a 12V dc output when the unregulated input voltage varies from 15V to 24V. When pass transistor is conducting, its collector to emitter saturation voltage is 0.5V. Assuming that the load is constant and the LC filter is ideal, find the minimum and maximum duty cycles of the pulse width modulator.
   (b) Write the Features and Applications of DC/DC converters [8+8]
2. (a) Derive the expression for the high 3-dB frequency f_h^* of n-identical non interacting stages in terms of f_H for one stage.
   (b) If four identical amplifiers are cascaded each having f_H =100 KHz, determine the overall upper 3dB frequency f_h^*. Assume non interacting stages.
   (c) Write a short note on Bootstrapped Darlington circuit. [5+5+6]
3. Draw the circuit diagram of a Double tuned amplifier and derive the expression for 3-dB bandwidth. [16]
4. (a) Define the terms:
      i. Load Regulation
      ii. Line Regulation
      iii. Ripple Rejection
      iv. Sense Voltage
   (b) In a zener diode regulator,
   Vi_{nom} = 40V, Vi_{min} = 35V, Vi_{max} = 45V V_z = 20V, r_z = 5 ohms I_{Lmin} = 0mA, I_{Lmax} = 100mA I_{zmin} = 10mA, I_{zmax} = 400mA. Find P_{zmax} and load resistance. [8+8]
5. (a) Show that in Hybrid - π model, the diffusion capacitance is proportional to the emitter bias current.
   (b) What is the frequency range to consider Giacolletto model of a transistor at high frequencies? What is the significance of f_T in discussing the frequency range of a transistor at high frequencies? [8+8]
6. (a) For a single stage transistor amplifier, R_S = 10K and R_L= 10K. The h-parameter values are $h_{fc} = -51$, h_{ic} =1.1KΩ, $h_{rc} \approx 1, h_{oc}$ = 25 μA/V Find A_I, A_V, A_{VS}, R_i, and R_o for the CC transistor configuration.

(b) For a single stage transistor amplifier, R_S=1KΩ, and R_L= 10K The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10^{-4}, h_{oe} = 25 μ A/V. Find A_I, A_V, A_{VS}, R_i, and R_o for the CE transistor configuration. [8+8]

7. Draw the circuit diagram of a class-B tuned amplifier. Explain its operation with neat waveforms. Also derive the expression for percentage efficiency and maximum power dissipation. [16]

8. (a) Draw the circuit of class -A series fed power amplifier and derive the expression for output power P_o. [10]

   (b) Draw and discuss the operation of Class - C power amplifier. [6]

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