# II B.Tech I Semester Examinations,November 2010 DIGITAL LOGIC DESIGN 

Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering
Time: 3 hours
Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks

* $\star \star \star \star$

1. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7 .
(b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v\& x
Mr.B has keys for locks v\& y
Mr.C has keys for locks w\& y
Mr.D has keys for locks $\mathrm{x} \& \mathrm{z}$
Mr.E has keys for locks $v \& z$
i. Determine the minimal no of executives required to open the safe.
ii. Find all the combinations of executives that can open the safe, write an expression $f(A, B, C, D, E)$ which specifies when the safe can be opened as a function of which executives are present
iii. Who is the 'essential executive' without whom the safe cannot be opened.

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[7+9]
$$

2. Convert the following numbers:
(a) 10101100111.0101 to Base 10
(b) $(153.513)_{10}=()_{8}$
(c) Find (3250-72532) ${ }_{10}$ using 10 's complement
(d) Divide 01100100 by 00011001
(e) Given that $(292) 10=(1204)_{b}$ determine ' $b$ ' $\quad[3+4+3+3+3]$
3. (a) Design a circuit with three inputs $(\mathrm{A}, \mathrm{B}, \mathrm{C})$ and two outputs $(\mathrm{X}, \mathrm{Y})$ where the outputs are the binary count of the number of "ON" (HIGH) inputs
(b) Design a circuit with four inputs and one output where the output is 1 if the input isdivisible by 3 or 7 .
4. Explain about HDL for Sequential Circuits in Detail?
5. (a) Draw and Explain the Gated-Latch Logic diagram
(b) Explain about the types of hazards in detail?
6. A DRAM chip uses two-dimenrtional address multiplexing. It has 13 common Address pins with the row Address having 1 bit longer than the column address. What is the capacity of the memory?
7. For the function $T(w, x, y, z)=\sum(0,1,2,3,4,6,7,8,9,11,15)$ :
(a) Find all prime implicants and indicate which are essential through the Kmap
(b) Design a circuit which will find the 2's complement of a 4 bit binary number.Use one full adder, 3 half adders and any additional gates.
[6+10]
8. Explain about 4-bit binary Ripple Counters?
[16]

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