Code No: 07A40402 **R07** **Set No. 2**

II B.Tech II Semester Examinations,December 2010
LINEAR IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Describe the principle of operation of precision half wave rectifier with waveforms.
   (b) Explain the operation of antilog amplifier using op - amp. [8+8]
2. (a) Draw a sample and hold circuit. Explain its operation with necessary input/output waveforms and indicate its uses.
   (b) Explain the operation of four-quadrant multiplier. [10+6]
3. Show with the help of circuit diagram an op - amp used as
   (a) scale changer
   (b) phase shifter
   (c) inverting adder and
   (d) non - inverting adder. Draw an op circuit whose output is $V_1 + V_2 - V_3 - V_4$. [16]
4. (a) An op - amp has a slew rate of $2V/\mu s$. What is the maximum frequency of an output sinusoid of peak value 5 V at which the distortion sets in due to the slew rate limitation?
   (b) What are the characteristics of an ideal op - amp and Explain. [8+8]
5. (a) Calculate the frequency of oscillation of a 566 VCO IC for the external component values R_T = 6.8kohms and C_T = 470PF. Assume other component values if necessary.
   (b) Draw the pin diagram of 566 VCO IC and list important specifications of 566 VCO IC. [8+8]
6. (a) Discuss about dc analysis of Dual input balanced output amplifier.
   (b) Why cascading is necessary for differential amplifier and explain its operation. [6+10]
7. Draw the functional block diagram of 555 IC timer. Explain the function of each block and also explain how it can be used as monostable multivibrator. Draw the circuit and explain its operation with neat relevant waveforms and derive the pulse width. [16]
8. (a) Explain the operation of an op - amp based weighted resistor Digital to Analog converter through a neat circuit diagram

(b) Design a 4 - bit weighted resistor DAC whose full-scale output voltage is 10 volts. Assume $R_f = 10$ kΩ and logic '1' level as +5 volts and also logic '0' level as 0 volts. What is the output voltage when the input is 1011? [8+8]

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Code No: 07A40402 **R07** **Set No. 4**

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LINEAR IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) What are the different types of multiplexers? Explain logic diagram and truth table of Dual 4 to 1 line multiplexer.
   (b) Explain the operation of balanced modulator using neat sketch. [10+6]
2. (a) Draw the circuit of Schmitt trigger using 555 timer and explain its operation.
   (b) How is an astable multivibrator using 555 timer connected in to a pulse position modulator. [8+8]
3. (a) Draw the circuit diagram and explain the operation of an inverting amplifier.
   (b) Derive the output voltage of an op - amp based differential amplifier. [8+8]
4. (a) Explain the design procedure (with suitable circuit diagram) of a fourth order Butter worth low pass filter.
   (b) A certain narrow band pass filter has been designed to meet the following specifications:
   f_c = 2kHz, Q = 20 and A_p = 10. What modifications are necessary in the filter circuit to change the center frequency 'f_c' to 1kHz, keeping the gain and band width constant? [10+6]
5. (a) Obtain differential mode gain of different configurations of differential amplifier using ac equivalent circuit.
   (b) Explain how level shifter acts as buffer to isolate high gain stages from the output stage. [8+8]
6. Derive the output voltage of an antilog amplifier and also explain its operation using op - amp circuit. [16]
7. (a) Draw the schematic circuit diagram of 4 bits Successive Approximation A/D converter and explain its operation.
   (b) Compare this A/D converter with Parallel comparator type A/D converter.
   (c) Describe the transfer characteristic of a Digital to Analog Converter.[8+4+4]
8. (a) What is the major difference between the power supply requirements of linear and digital Ics?
   (b) Explian the Pole - Zero and Dominant pole compensation techniques for an op - amp. [6+10]

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II B.Tech II Semester Examinations,December 2010
LINEAR IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the following in detail:
   i. Phase comparator
   ii. VCO
   (b) What is the role of LPF in PLL
   (c) Give any two applications of PLL and explain in detail. [6+4+6]
2. Write short notes on:
   (a) IC 1496 and its applications
   (b) Sample and hold circuit. [16]
3. (a) What is meant by DC coupling?
   (b) Discuss the operation of single ended input and unbalanced output differential amplifier.
   (c) Calculate V_2 for the level shifter shown in figure 3. Assume identical silicon transistors with $V_{BE} = 0.705$V and $\beta = 100$ and V_1 of 12V. [4+8+4]

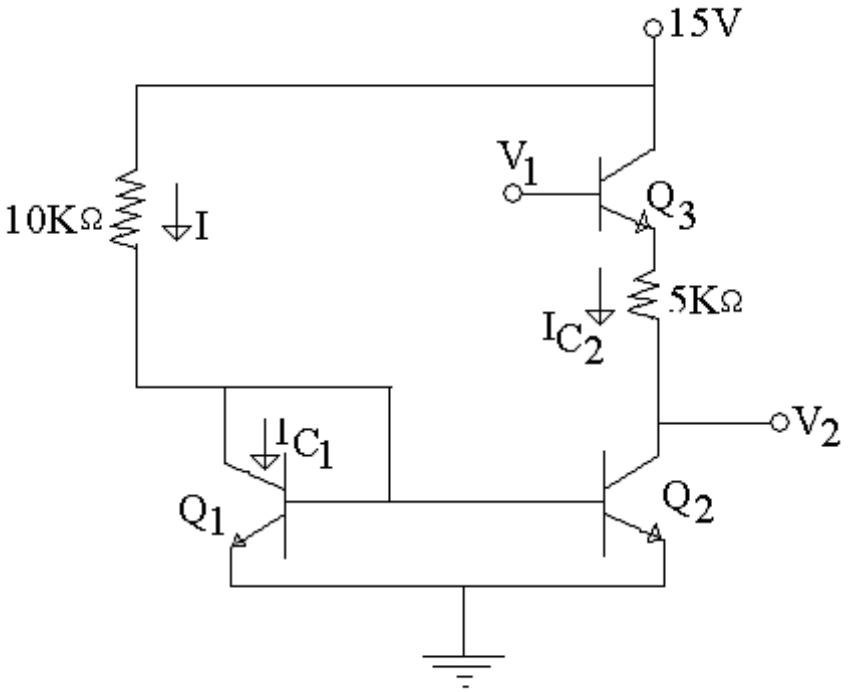

Figure 3

4. (a) For the non - inverting a.c. amplifier $R_{in} = 50\Omega$, $c_i = 0.1\mu f$, $R_1 = 1K\Omega$,$R_0 = R_3 = 820\Omega$, $R_F = 5.6K\Omega$ and $R_l = 10K\Omega$. Determine the gain and band width of the amplifier.

   (b) What is an instrumentation amplifier? List any three applications of the instrumentation amplifier. [8+8]

5. (a) For the all pass filter, determine the phase shift ϕ between the input and output at f = 2kHz. To obtain a phase shift ϕ , what modifications are necessary in the circuit?

   (b) Derive the expression for the transfer function of 2nd order High pass filter. [8+8]

6. (a) What is a precision diode?

   (b) Draw the circuit of a negative peak clamper and explain its operation with necessary waveforms.

   (c) Explain the functioning of a peak detector with necessary diagrams. [2+8+6]

7. (a) Compute the maximum possible total output voltages in the amplifier circuits shown in figure 7. The op - amp is the MC1536 with the following specifications:
   $V_{io} = 7.5mV$ maximum; $I_{io} = 50nA$ maximum; $I_B = 250$ nA maximum at $T_A = 25^0C$.

   (b) Explain the difference between the slew rate and the transient response.

   (c) Briefly explain the need for compensating networks in op - amps. [4+6+6]

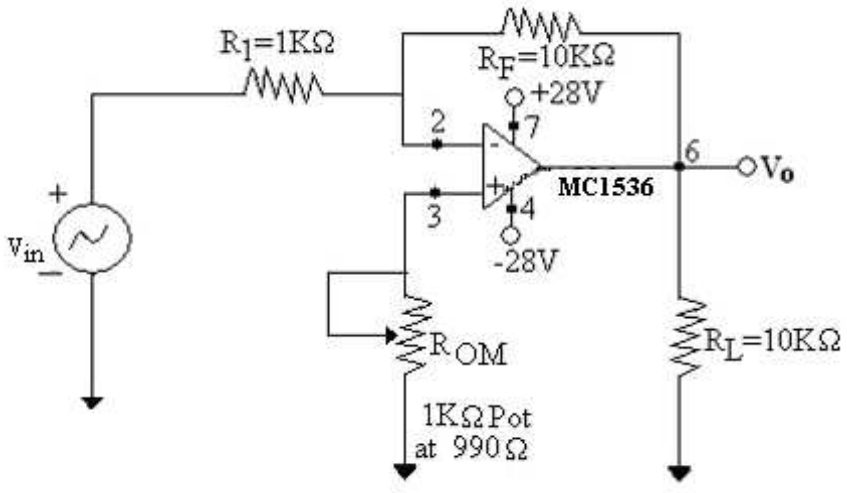

Figure 7

8. (a) Sketch and explain the transfer characteristic of a DAC with necessary equations.

   (b) LSB of a 9 - bit DAC is represented by 19.6mv. If an input of 9 zero bits is represented by 0 volts.

      i. Find the output of the DAC for an input 10110 1101 and 01101 1011.

ii. What is the Full scale reading (FSR) of this DAC? [8+8]

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1. (a) Draw the circuit of a 4 bit binary weighted resistor type DAC and explain its operation.
   (b) Explain the operation of dual slope ADC with neat diagram and waveforms. [8+8]
2. (a) What is an op-amp? Why it is called so?
   (b) Explain the parameters that should be considered for ac and dc applications of an op-amp.
   (c) Draw and explain the three open loop op - amp configurations with neat circuit diagram. [4+7+5]
3. (a) Draw the circuit of PLL as frequency multiplier and explain its working.
   (b) Explain with neat diagram how 555 timers can be used as a Schmitt trigger. [8+8]
4. (a) Explain how multiplier can be used to modulate and demodulate an AM signal.
   (b) What is meant by balanced modulator? Explain its function using neat diagram. [8+8]
5. (a) Explain how an op - amp can be used as summing amplifier? Draw the diagram of a four input summer and obtain the expression for the output.
   (b) The circuit of a inverting summing amplifier is designed with $R_1 = R' = 1$Kohm, and $R_2 = 2R_1$, $R_3 = 2R_2$..Rn = $2R_{n-1}$, the input voltages $v_1, v_2 ... v_n$ can be 0 to 10V.
      i. For n = 4, what is the smallest output voltage if at least one input is nonzero?
      ii. For n = 4, what is the maximum output voltage? [8+8]
6. (a) Why is emitter resistor R_E replaced by a constant current bias circuit in differential amplifier stage of an op - amp.
   (b) Classify different Ics.
   (c) Derive the expression for CMRR for the first stage differential amplifier. [6+3+7]
7. (a) Determine the order of a low pass Butterworth filter that is to provide 40 dB attenuation at $\omega/\omega_h = 2$.

(b) What are the different configurations of notch filter? Explain in detail with suitable circuit diagram. [4+12]

8. (a) Design a logarithmic amplifier for positive input voltages in the range 5mV to 50V.

(b) With suitable circuit diagram explain the operation of a triangular wave generator using a comparator and a integrator. [8+8]

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