Code No: 07A4EC02 **R07** **Set No. 2**

II B.Tech II Semester Examinations,December 2010
LINEAR AND DIGITAL IC APPLICATIONS
Common to Instrumentation And Control Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Explain Functional diagram of successive approximation ADC
   (b) Explain counter type A/D converter. [8+8]

2. (a) Describe the 555 timer Monostable multivibrator applications in
      i. Frequency Modulation.
      ii. Pulse Width Modulation.
   (b) Describe
      i. Pulse Position Modulation (PPM) and
      ii. FSK generator
      using 555 timer astable multivibrator. [4+4+8]

3. (a) Sketch ROM cells using BJT and MOS for storing 0 and 1.
   (b) Explain how memories are used in Microprocessor based systems. [8+8]

4. (a) Explain the classification of integrated circuits
   (b) Sketch TTL NAND Gate and explain its working
   (c) Sketch TTL NOR Gate and explain its working. [4+6+6]

5. (a) Calculate the frequency of oscillation of a 566 VCO IC for the external component values $R_T = 6.8K\Omega$ and $C_T = 470PF$. Assume other component values if necessary shown in figure 5a.
   (b) Derive the expression for frequency of VCO and list important specifications of 566 VCO IC. [8+8]

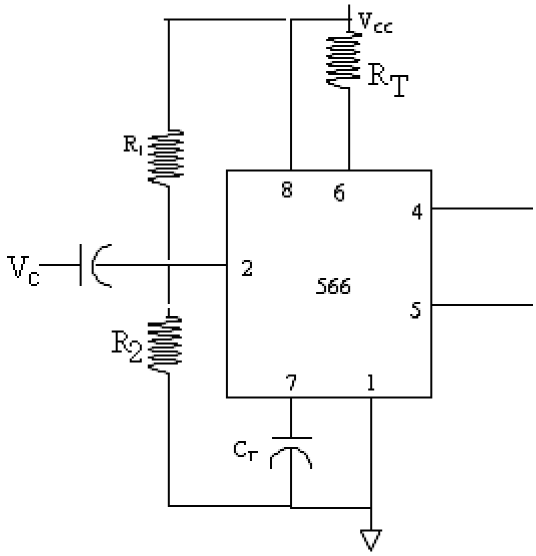

Figure 5a

6. (a) Discuss the operation of a log amplifier and derive the expression for output voltage.

   (b) Design a current to voltage converter using Op-amp and explain how it can be used to measure the output of a photocell. [8+8]

7. Explain and design the leading zero suppression using BCD / 7- segment display. [16]

8. (a) Explain the terms:

   i. CMRR.
   ii. PSRR.
   iii. Thermal drift.
   iv. Inverting configuration of Op-Amp.

   (b) The 741IC Op-amp having the following amplifier with $R_1 = 1K\Omega$, and $R_F = 10k\Omega$, A=200000, $R_i = 6\ M\Omega$, $R_o = 150\ \Omega$, $f_o = 5$ Hz, Supply voltages = ± 15 V, O/P Voltage Swing = ± 13V. Compute the values of

   i. A_F closed loop voltage gain.
   ii. f_F bandwidth with feedback.
   iii. Input resistance.
   iv. Output Resistance. [8+8]

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Code No: 07A4EC02 **R07** **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Specify the following parameters for 74 TTL
   (a) I_{OL}(max)
   (b) I_{OH}(max)
   (c) I_{IL}(max)
   (d) I_{IH}(max). [4+4+4+4]

2. (a) What do you mean by don't care combinations?
   (b) What you mean by min terms and max terms of Boolean expressions.
   (c) Simplify the Boolean function using K-map
   $F = \sum m(0, 1, 3, 4, 5, 6, 7, 8, 9)$+dontcare$(10, 11, 12, 13, 14, 15)$ [4+4+8]

3. (a) Draw the schematic circuit diagram of the following and explain their working.
      i. Analog phase detector.
      ii. VCO.

   Derive necessary expressions.
   (b) What is their role is in PLL? Explain. [6+6+4]

4. (a) An op-amp has a slew rate of $2V/\mu s$. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation. Derive the formulae used.
   (b) If the sinusoid of 10V peak is specified, what is the full power band width?
   (c) List out the non ideal DC characteristics of an Op-amp? [8+4+4]

5. (a) Define the conditions on the feedback circuit of an amplifier to convert it in to an oscillator.
   (b) Design an RC phase shift oscillator for 300HZ frequency using IC μA 741 and $\pm$15V power supplies. Assume necessary component values.
   (c) Suggest a method to reduce the output voltage swing to I $\pm$ 6.5 Volts.[6+6+4]

6. (a) Explain the operation of zero crossing detector using Op-amps.
   (b) Design a differentiator using Op-amp to differentiate an input signal that varies in frequency from 1 KHz to 10 KHz. [8+8]

7. Explain and design the trailing zero suppression using BCD / 7- segment display. [16]

8. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000000000000 represents 0V, what output is produced if the input is 1101101111111111?

   (b) Calculate the values of the LSB, MSB and full scale output for an 32 bit DAC for the 0 to 20V. [8+8]

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Code No: 07A4EC02 **R07** **Set No. 1**

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Time: 3 hours Max Marks: 80

Answer any FIVE Questions
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1. Design 4:1 Mux with logic diagram and symbolic representation. [16]

2. (a) Define by means of a diagram the pass band, stop band, transition band and pass band ripple.
   (b) Sketch the ideal frequency-response characteristics of Low pass, high pass and band reject filters.
   (c) Design a second order low pass filter at a higher cut off frequency of 2KHz. [5+5+6]

3. Write short note on:
   (a) R-2R Ladder DAC
   (b) inverted R-2R Ladder. [8+8]

4. (a) Explain with neat sketch how four bits 1110 are serially entered into the shift register.
   (b) Explain with neat sketch how four bits 1110 are serially shifted out of the shift register. [8+8]

5. (a) Classify the types of Op-amp based multipliers. How a multiplier can be used to
      i. Double the incoming frequency.
      ii. Detect the phase angle of a signal.
   (b) Design a subtractor in non inverting configuration. [8+8]

6. (a) Discuss any two applications of 555 timer in Monostable mode.
   (b) Design a square waveform generator of frequency 1kHz and duty cycle of 75% using 555 timer. [10+6]

7. (a) Sketch CMOS NAND Gate and explain its working
   (b) Sketch CMOS NOR Gate and explain its working. [8+8]

8. (a) What are the three differential amplifier configurations? Compare and contrast these configurations.
   (b) What is a level translator circuit? Why is it used with the cascaded differential amplifier used in Op-amps?

(c) Explain the term "Slew Rate" and how it affects the frequency response of an Op-amp? [10+3+3]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Convert the binary numbers to gray codes using Ex- OR gates
   (a) 1001
   (b) 11001111
   (c) 10000001
   (d) 10011 [4+4+4+4]

2. Explain the following terms:
   (a) $I_{OL(max)}$
   (b) $I_{OH(max)}$
   (c) $I_{IL(max)}$
   (d) $I_{IH(max)}$ [4+4+4+4]

3. (a) What is a clipper? With circuit diagram, explain the operation of positive and negative clippers.
   (b) Describe the principle of operation of a precision half wave rectifier with wave forms. [10+6]

4. (a) Explain the role of the basic building blocks of PLL.
   (b) Determine the DC control voltage v_c at lock if signal frequency f_s = 10 KHz, VCO freerunning frequency is 10.66 KHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz / V. [10+6]

5. (a) Draw the circuit diagram and explain the operation of an inverting amplifier, obtain the expression for closed loop voltage gain.
   (b) Derive the output voltage of an Op-amp based differential amplifier. [8+8]

6. (a) Define Bessel, Butterworth and Chebysher filters, and compare their frequency response.
   (b) Sketch the block diagram of I/II order band elimination filter and design a I order wide band- reject having f_H=200 Hz and f_L =1 kHz, having the passband gain of 2 each. Assume necessary data. [6+10]

7. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000011111111 represents 0V, what output is produced if the input is 1111111111011011?

(b) Calculate the values of the LSB, MSB and full scale output for an 32bit DAC for the 0 to 20V. [8+8]

8. (a) Draw five stage synchronous binary counter using D flip flop.

(b) Draw complete timing diagram for the same. [8+8]

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