Code No: 07A4EC09 **R07** **Set No. 2**

II B.Tech II Semester Examinations,December 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the procedure for the following with an example
   (a) Conversion from Binary to decimal number
   (b) Binary subtraction using 1's complement
   (c) Binary subtraction using 2's complement
   (d) Conversion from gray to binary number [16]

2. Design an arithmetic circuit that adds 2 binary digits. The circuit should have 2 outputs, one for the sum and the other for the carry. Implement the same in a PAL. [16]

3. Implement the following functions using appropriate DECODER
   F1 = Σm(2,4,6,8,12)
   F2 = Σm(1,3,6,7,9,10)
   F3 = Σm(1,3,4,5,6,9,12,14)
   F4 = Σm(2,4,8) [16]

4. For the machine shown, find the equivalent partition and a corresponding reduced machine in standard form. [16]

PS	NS,Z	
	X = 0	X = 1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

5. Simplify the following to least number of literals using Boolean Algebra
   (a) AB′CD′ +ABD′+BCD′+A′B+BC′
   (b) X+XY′Z+X′YZ+XW+XW′+X′Y
   (c) (AB+A′C+BC)(A+B′+AB′)
   (d) (A+B+C′)(A+B′+C′)(A′+B+C′)(A′+B′+C′) [16]

6. Design the ASM chart, Data path circuit & Control circuit to implement traditional division of two four bit binary numbers. [16]

7. Design a combinational logic circuit that has 5 inputs, The output is required to go HIGH whenever the number of inputs have odd number of 1s. Draw the Truth table. Minimize the Boolean function using K-map. Draw the circuit diagram. [16]

8. Design a 4 bit counter that counts either in Binary or gray depending on the input given to the select line. When select line = 0, the counter is to count in Binary, and when select line = 1, the counter is to count in gray. Draw the logic diagram. [16]

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Code No: 07A4EC09 **R07** **Set No. 4**

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1. (a) Design a combinational logic circuit using ROM. The circuit accepts BCD number and generates an output binary number equal to the 2s complement of the input number.
   (b) Explain advantages of Mask programming. Give the Hardware procedure for PROMs and EPROMs. [8+8]

2. Design a synchronous sequential circuit of a full subtractor. Design the ASM chart to implement the above mentioned design. Design the data processing unit and control unit using PLA control. [16]

3. Prove the following identities by writing the truth tables for both sides:
   (a) X.(Y + Z) = (X.Y) +(X .Z)
   (b) (X.Y.Z)′ = X′ + Y′ +Z′
   (c) X.(X +Y) = X
   (d) X + X′Y = X + Y [16]

4. Construct the compatibility graph and obtain the minimal cover table for the incompletely specified sequential machine specified in the state table given below. [16]

PS	NS,Z	
	J1=0	J2=1
A1	-	A6,0
A2	A2,0	A3,0
A3	A5,0	A1,1
A4	A2,0	A4,0
A5	A6,1	A4,0
A6	A1,0	-

5. Map the following function and simplify using K-Map
   (a) F = (A+B+C)(A+B′+C)(A+B′+C′)(A′+B+C)
   (b) F = (A′BC′D′+A′BC′D+AB′CD+AB′CD′+ABCD+A′B′C′D′) [16]

6. (a) Design a Serial in and parallel out 4 bit Shift Register.
   (b) Design a 8-bit Ring counter. [8+8]

7. (a) Convert the following decimal numbers to BCD and perform BCD addition
   i. 14 + 20
   ii. 10 + 22
   iii. 24 + 60
   iv. 44 + 55
   (b) Write short notes on Excess-3 codes [12+4]

8. Design a 32 to 1 Multiplexer. Implement the following switching function in a mux
   F = Σm(1,3,5,6,7,9,10,12,14,18,21,25) [16]

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Code No: 07A4EC09 **R07** **Set No. 1**

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1. Explain the design procedure of
   (a) Multiplexer
   (b) Half adder
   (c) MSI devices [16]
2. Simplify the following function using Tabulation method and verify the result using K-map
   (a) F = Σm(0,1,2,4,6)
   (b) F = Σm(1,3,5,7,9,10,12,15)
   (c) F = Σm(3,5,7,9)
   (d) F = Σm(1,2,6,10,11) [16]
3. (a) Draw an ASM chart to convert D-Flip flop to T flip flop.
   (b) Give the procedure to design a data processing unit and a control unit [8+8]
4. (a) Write short notes on Asynchronous inputs.
   (b) What is excitation table? Write the excitation tables for the following flip flops
      i. SR Flip flop
      ii. JK flip flop
      iii. D flip flop
      iv. T flip flop [4+12]
5. (a) Justify why computers use binary codes
   (b) Write short notes on weighted codes and Un-weighted codes with suitable examples
   (c) Encode each of the 10 decimal digits 0,1,2,3,4,5,6,7,8,9 by means of the following weighted binary codes:
      i. 5 4 -2 -1
      ii. 7 3 2 -1 [4+4+8]
6. The state table of a sequential machine is shown below. Obtain the compatibility graph using.

(a) Merger graph

(b) Merger Table [16]

PS	NS,Z	
	Y = 0	Y = 1
A	F,0	A,0
B	E,0	C,0
C	C,-	B,0
D	F,1	D,0
E	A,1	C,0
F	D,-	F,0

7. Design a 4 input priority encoder in a ROM and PAL. [16]

8. (a) Convert the following SOP equation into its POS form.
G = XY′Z + X′YZ′

(b) Reduce the following Boolean expressions to three literals.
A′C′ + ABC +AC′ 8+8]

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1. (a) Define the following terms
   i. Boolean function
   ii. Sum of products form
   iii. Product of sum form
   iv. Dont care conditions
   (b) Convert the following expressions into their respective canonical forms
   i. WY + W′XZ +WYZ′
   ii. (W + X +Y′) (W +Z)

   [8+8]

2. Design a synchronous sequential circuit which has control unit C, clock and outputs x, y and z. If C=1, on every rising edge of the clock, code on output x, y and z changes from 111 → 000 → 010 → 100 → 111 and repeats. Design the ASM chart to implement the above mentioned design. Design the control unit using PLA control. [16]

3. Solve for X
   (a) $(AE232)_{16} = (X)_{10}$
   (b) $(5CA2)_{16} = (X)_3$
   (c) $(1.234)_{10} = (X)_8$
   (d) $(3232)_8 = (X)_{10}$ [16]

4. (a) Define the function of a decoder. Design a 3 to 8 decoder. Draw the circuit diagram, function table and explain the working of the decoder circuit.
   (b) Design a Decimal to BCD decoder. [8+8]

5. Find the equivalence partition for the machine shown below.
   Show a standard form of the corresponding reduced machine. [16]

PS	NS,Z	
	X = 0	X = 1
A	E,0	C,0
B	C,0	A,0
C	B,0	G,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0

6. Explain the construction of Master slave flip flop. Explain the procedure of Master slave flip flop using JK flip flop. Explain with waveforms. [16]

7. List the PLA Programming table for OCTAL to BCD converter. Implement the function in a ROM and PLA. Compare both the design and justify which is the most economical. [16]

8. Design a logic circuit with 4 inputs. The circuit should produce a 1 at its output when the excess-3 equivalent of the input consists of even number of 1's.Use K-map for minimization of the switching function. [16]

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