Code No: 07A4EC13 **R07** **Set No. 2**

II B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
2. (a) What is pipeline? Explain. [8]
   (b) Explain arithmetic pipeline. [8]
3. (a) Compare communication costs in multicomputer and multiprocessor systems.
   (b) Explain about Amdhal's Law. [10+6]
4. Explain about BUN (branch unconditionally), BSA (branch and save return address), and ISZ (increment if zero) operation. Explain which of the processors registers will be in executing the above control operations. [4+8+4]
5. (a) Explain non restoring method of division with a simple example. [8]
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8]
6. What is a priority Interrupt? Explain various Interrupt handling methods? Explain. [16]
7. Draw a block diagram of a control memory with associated HW for finding out next microinstruction address. Clearly specify the control flow. What is meant by mapping process in this context? [16]
8. (a) Explain multiport memory organization with a neat sketch.
   (b) Explain system bus structure for multiprocessors with a neat sketch. [8+8]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Explain the following with applications for each:
   (a) ROM
   (b) PROM
   (c) EPROM
   (d) EEPROM. [4+4+4+4]
2. (a) What is a pipeline register. What is the use of it? Explain in detail. [8]
   (b) Why do we need some bits of current microinstruction to generate address of the next microinstruction. Support with a live example. [8]
3. (a) Give some examples for register reference, memory reference, logical, shift, I/O and branch instructions. [10]
   (b) What is the use of buffers? Explain about tri-state buffers. Explain about high impedance state. [6]
4. (a) Explain bit oriented and character oriented protocols in serial communication.
   (b) What are the different issues behind serial communication? Explain. [8+8]
5. (a) What is pipeline? Explain space-time diagram for Pipeline.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]
6. (a) Is it possible to improve every program by using more than one processor?. Give one supporting example? [8]
   (b) Compare multicomputers and multiprocessors. [8]
7. (a) What are the total number of switches in a 8×8 omega network? Show a neat sketch.
   (b) How many nodes will be there in a 4 Dimensional hyper cube? Show a neat sketch [8+8]
8. Explain the basis for booths multiplication algorithm along with its constituents steps. What type of numbers it will work?. What are the limitations of the same. What are the HW requirements to realize the same in HW. Give an example for the working of Booth?s algorithm. [16]

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Code No: 07A4EC13 **R07** **Set No. 1**

II B.Tech II Semester Examinations,December 2010
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Multiply 10111 with 10011 using, Booths algorithm. [8]
   (b) Explain booths algorithm with its theoretical basis. [8]
2. (a) Explain the functioning of hypercube network with an example. Show a neat sketch
   (b) Explain the working of omega switching network. Show a neat sketch. [8+8]
3. (a) Differentiate between microprogramming and nanoprogramming. [8]
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [8]
4. (a) Explain the terms NaN, overflow and underflow in the IEEE 754 representation of floating point numbers.
   (b) Explain 2's complement method of representing numbers. When can you say that an overflow has occurred when adding or subtracting two fixed point numbers.
   (c) What do you mean by a parity bit? Explain with an example how even and odd parity bits are generated. Is it possible to correct errors using parity bits. [6+5+5]
5. (a) Differentiate RISC and CISC computers.
   (b) Expalin RISC pipelining. [8+8]
6. (a) Explain how the Bit Cells are organized in a Memory Chip. [8]
   (b) Explain the organization of a 1K x 1 Memory with a neat sketch. [8]
7. (a) What are various Peripheral Devices used in computer system? Explain.
   (b) What is the need of I/O Interface? Explain. [8+8]
8. (a) Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Give 8-bit examples. [10]
   (b) Design a circuit for combined shift left/right operations. Assume register length is 4 bits and employ RS employ flip-flops. [6]

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Code No: 07A4EC13 **R07** **Set No. 3**

II B.Tech II Semester Examinations,December 2010
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers. [8]
   (b) Multiply 10111 with 10011 with the above procedure given (a). Show all the registers content for each step. [8]
2. (a) Explain RISC pipeline in detail.
   (b) Explain vector processing. [8+8]
3. (a) Explain the various microinstruction encoding techniques. [8]
   (b) List and explain the implicit microinstruction address generation techniques. [8]
4. Mention about full adder circuit functionality with inputs and outputs using a block diagram. Using FA blocks design combined adder cum subtractor circuit. Assume two numbers are 4-bit numbers. [16]
5. (a) Explain the functioning of omega switching network with a neat sketch. [8]
   (b) In 8 x 8 omega switching network how many stages are there and in each stage how many Switches are there. [4]
   (c) How many stages and how many Switches in each stage are needed in a n x n omega sitching network. [4]
6. Explain the following:
   (a) CPU - I O P Communication
   (b) I O P
   (c) IBM 370 I/O Channel. [5+5+6]
7. (a) Explain the terms computer architecture, computer organization and computer design in a detailed fashion. [8]
   (b) Explain about MIPS, FLOPS rating of a processor. How do we arrive at these values. [8]
8. (a) How to implement 2K x 32 memory module using 512K x 8 static memory chips? Show a neat sketch. [8]
   (b) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes? [4]

(c) How many lines of address bus must be used to access 2048 bytes of memory? [4]

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