Code No: 07A50402 **R07** **Set No. 2**

III B.Tech I Semester Examinations,November 2010
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) With the help of transfer characteristics, input and output wave forms explain the operation of non-inverting Schmitt trigger circuit.
   (b) What is sample and hold circuit? Explain its operation with the help of circuit diagram and waveform. [8+8]
2. (a) Explain how dual supply operation is obtained from single supply connection.
   (b) Explain various stages through the internal block diagram of an op-amp.[8+8]
3. (a) List the advantages of current mirror circuit when it is used as active load or constant bias circuit.
   (b) Explain the meaning of Balanced and unbalanced outputs and Single and Dual ended inputs. [8+8]
4. (a) Discuss the performance parameters of sample & hold circuits in detail.
   (b) What are the advantages of sample & hold circuit. [8+8]
5. (a) An IC555 timer used as a monostable has R=20 KΩ and C = 0.01μf. What is the duration of output pulse?
   (b) Explain how IC555 can be used as missing pulse detector. [8+8]
6. (a) Explain the operation of voltage to current converter.
      i. With floating load
      ii. Grounded load.
   (b) An inverting amplifier using op-amp has R_1 = 10 kΩ and R_f = 47 KΩ. It is applied with 2V peak to peak sine wave. An AC voltmeter is used between the output terminal and ground to measure the output voltage calculate the reading on the voltmeter. Assume supply voltage to be ± 12V. [8+8]
7. (a) Draw the circuit and explain the operation of narrow band pass filter.
   (b) Design a narrow band pass filter with two feed back paths with F_c=1.5KHz Q=7 and A_F=15. [10+6]
8. (a) Compare the conversion times and efficiencies of 8-bit tracking type and successive approximation type A/D converters.
   (b) Determine the resolution of an 8-bit A/D converter for a 10V input range.
   (c) If the maximum output voltage of a 7-bit D/A converter is 25.4 V. What is the smallest change in the output as the binary count increases. [6+6+4]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A50402 **R07** **Set No. 4**

III B.Tech I Semester Examinations,November 2010
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Suggest different methods to increase the input resistance of an op-amp.
   (b) Compare the four configurations of differential amplifier with reference to the parameters A_d, A_C, R_{in} and R_o, CMRR. [8+8]

2. (a) Explain the operation of +ve and -ve clampers with suitable sketches.
   (b) What are the application of comparator? Explain. [8+8]

3. (a) Draw and explain the functional block diagram of IC 555.
   (b) Explain the functioning of 555 in Monostable configuration. [8+8]

4. (a) Draw the circuit and explain the operation of wide band reject filter.
   (b) Design a wide band reject filter having f_H= 400 Hz and f_L= 2KHz with a pass band gain of 2. [10+6]

5. (a) Explain the operation of balanced modulator using diodes.
   (b) Briefly explain the following.
      i. Square circuit.
      ii. Square rooting circuit. [8+8]

6. (a) What is an ideal active integrator? Explain its working with neat circuit diagram.
   (b) Design a practical integrator circuit with a D.C. gain of 10, to integrate a square wave of 10 KHz. [8+8]

7. (a) Compare dominant pole and pole-zero compensation technique.
   (b) In the amplifier circuit shown in figure 1 $R_1 = 100\Omega$ $R_f = 4.7$ KΩ, CMRR = 90dB. If the amplitude of the induced 60 Hz noise at the output is 5V (rms) calculate the amplitude of the common mode input voltage V_{cm}. [8+8]

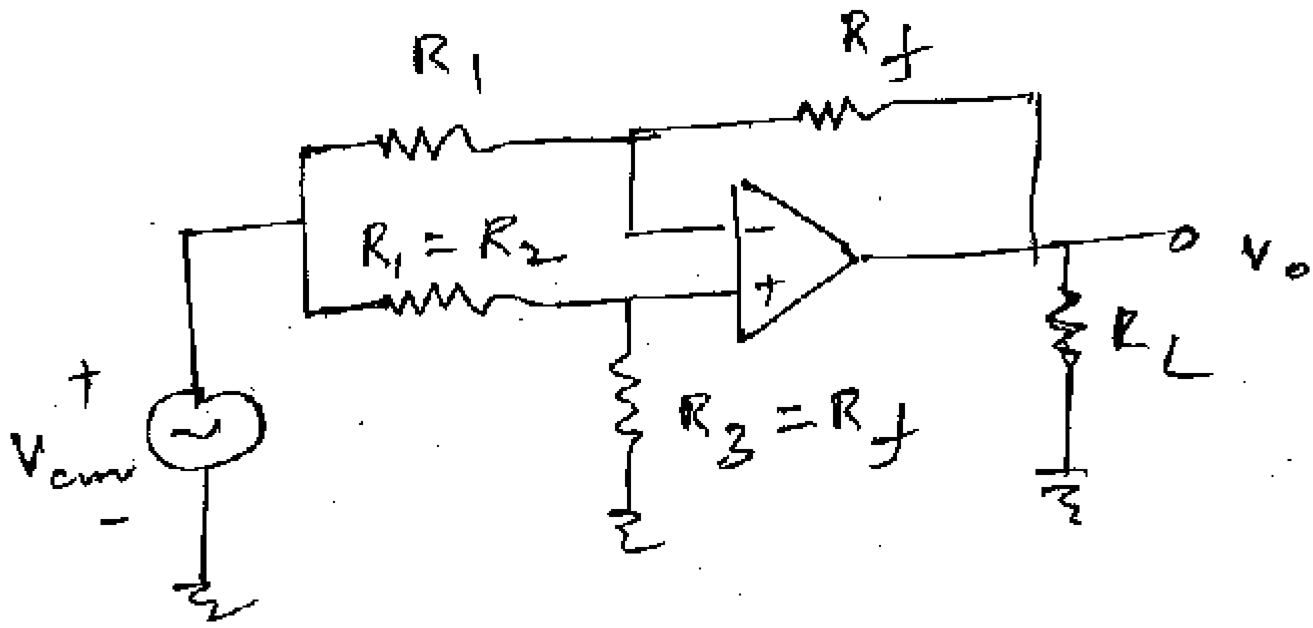

Figure -1

8.(a) Discuss the features operation and pin diagram of 0803 and 0808 .

(b) Calculate the quantizing error for 12-bit ADC with full scale input voltage 4.095V.

[8+8]

****

Code No: 07A50402 **R07** **Set No. 1**

III B.Tech I Semester Examinations,November 2010
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Define and explain the following performance parameters of a multiplier.
   i. Accuracy
   ii. Linearity
   iii. Bandwidth
   iv. % absolute error bandwidth
   v. Feed through voltage
   vi. Zero trim
   vii. Scale factor. [16]

2. (a) Explain the operation of 1^{st} order low pass filter.
   (b) What are the design steps for the 1^{st} order low pass butter worth filter.
   (c) What is frequency scaling? Explain. [6+6+4]

3. (a) What is active load? Where is it used? Explain the necessity of active loads.
   (b) What are the methods of obtaining high input resistance for the differential amplifier circuit? Explain. [8+8]

4. (a) Explain the operation of phase detector using XOR gate. Draw input and output wave forms.

   (b) Show that the lock-in range of a PLL is given by $\Delta f_L = \pm 7.8 f_0/V$. Where the symbols used have the usual meaning. [10+6]

5. (a) Explain the operation and derive the expression for the overall gain of the three op-amp instrumentation amplifier. What are its advantages.

   (b) If $R_1 = R_2 = 5$ KΩ in a three op-amp instrumentation amplifier, determine the value of external resistance R_G required to get the gain of 300. [8+8]

6. (a) Explain how the following op-amp parameters are measured.

      i. Open loop voltage gain.
      ii. Input bias current.
      iii. Input offset current.
      iv. Input offset voltage.

   (b) An op-amp has a slew rate of 2V / μS. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets is due to the slew rate limitation. [8+8]

7. (a) Draw the timing wave forms of ADC 0808.

   (b) Compare Dual slope type, Flash type successive approximation register type and counter type ADCs interms of conversion times and accuracies. [8+8]

8. (a) Explain the operation of temperature compensated transistor used log amplifier. Derive the expression forV_0. What are its drawbacks?

   (b) Describe frequency compensated log amplifier. [8+8]

⋆⋆⋆⋆⋆

Code No: 07A50402 **R07** **Set No. 3**

III B.Tech I Semester Examinations,November 2010
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are the important features of counter type A/D converter.
   (b) Compare tracking and counter type converters.
   (c) Determine the resolution of a 8-bit A/D converter for a 10V input range. [6+6+4]

2. Obtain the expressions for A_d, A_c, R_i and R_0 for dual input unbalanced output differential amplifier configuration. [16]

3. (a) Explain how op-amp can be used as comparator. Draw and explain the operation of basic non-inverting comparator circuits with the help of transfer characteristics and waveforms.
   (b) For the figure 3 as shown in, calculate the values of R_1 and R_2 if saturation voltages are +12V and -12V. Assume hysteresis width = 6V. [8+8]

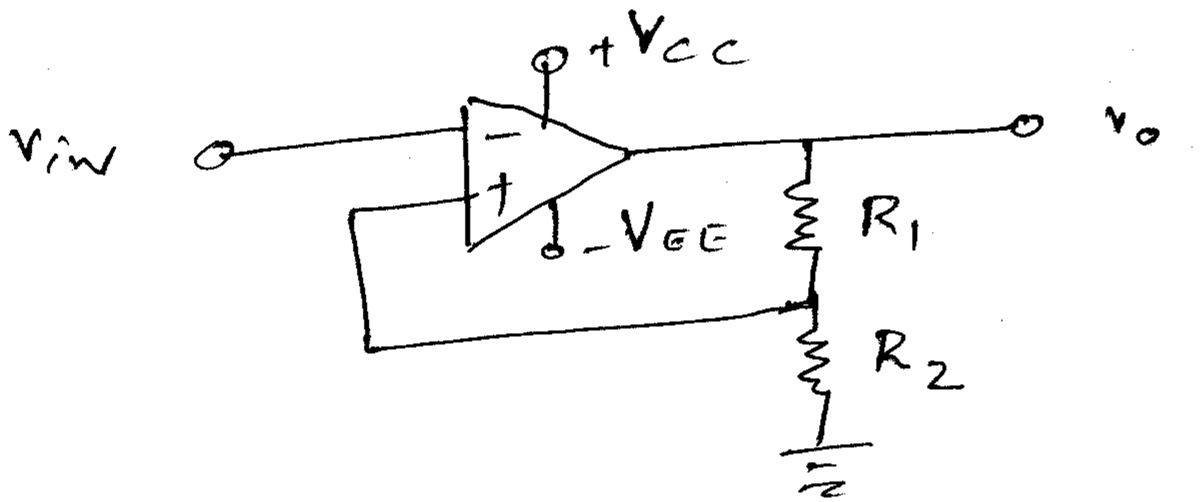

Figure 3:

4. (a) What is an all-pass filter? Explain its operation and application areas.
   (b) For the all-pass filter, the value of R and C are 7.95 KΩ and 0.02 μf respectively. If the input frequency is 1.5 KHz calculate the phase shift. [10+6]

5. (a) List the parameters to be considered while selecting the op-amp for a particular application.

(b) What are the absolute maximum ratings of the commercial op-amp? Explain. [8+8]

6. (a) Derive the expression for the frequency of the output of an astable multivibrator.

(b) A 555 timer is configured to run in astable mode with R1 = 20KΩ and R2 = 8KΩ and C = 0.1μf. Determine the output frequency and duty cycle. [8+8]

7. (a) Draw the basic logarithmic multiplier circuit and explain how it multiplies two voltages

(b) With the neat circuit diagram explain the operation of an op-amp based sample & hold circuit. [8+8]

8. (a) With the help of suitable circuit diagrams show that an op-amp can be used as:

i. Scale changer
ii. Phase shifter
iii. Inverting adder
iv. Non inverting adder.

Draw an op-amp circuit whose output is $V_1 + V_2 - V_3 - V_4$

(b) For the practical inverting amplifier, the values of R_f and R_1 are 470 Ω and 4.7KΩ various specification for the op-amp used are open loop gain = 2×10^5. Input resistance = 2 MΩ Output resistance = 75Ω since break frequency = 5Hz. Supply voltages = $\pm$ 15V, calculate the closed loop voltage gain, input resistance, output resistance and bandwidth with feedback. [16]

⋆⋆⋆⋆⋆