

Code No: 07A50403

R07**Set No. 2****III B.Tech I Semester Examinations, November 2010****DIGITAL IC APPLICATIONS****Electronics And Communication Engineering****Time: 3 hours****Max Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. Generate the truth table and draw the circuit diagram for
 - (a) Dual parity generator for an 8-bit input
 - (b) 4-bit magnitude comparator. [16]
2. (a) Explain briefly about behavioral design elements.
 (b) Explain about time Dimension. [8+8]
3. What are the Relational operators and Equality operator? Give examples and explain about them. [16]
4. (a) Draw the circuit diagram and function table of a positive edge triggered commercial D flip-flop which is similar to one of the two flip-flops on an MSIIC 74x74.
 (b) What is a scan flip-flop? Draw the extra logic necessary to convert a normal flip-flop into a scan flip flop. Draw its function table and logic symbol. [8+8]
5. Compare DTL, TTL and CMOS logic families, giving typical values of various parameters. [16]
6. (a) Draw the internal structure of a MOS transistor based Read only memory. Describe the procedure to fuse a combinational circuit in to this type of ROM with the help of a simple example.
 (b) Discuss whether it is possible to build a ROM using bipolar Junction transistors?
 (c) List out the merits and demerits of the above three types of ROM. [5+5+6]
7. (a) Explain about the terms
 - i. Fan-in
 - ii. Fan-out
 - iii. Noise margin
 - iv. Propagation delay
 (b) Draw the circuit for CMOS NAND and clearly explain about its functioning. [8+8]
8. (a) Draw the truth table for implementing a 3-to-8 decoder similar to 74X138 MSI chip. Use one active low enable input $\bar{G}$ and active high outputs, y_7 to y_0 . Convert the truth table into suitable dataflow model of VHDL code.

Code No: 07A50403

R07**Set No. 2**

- (b) Construct the function, $F(w_3, w_2, w_1) = \sum m(0, 1, 3, 4, 6, 7)$
by using a 3-to-8 decoder and an OR gate. Draw the circuit diagram for the
function representing 3-to-8 decoder as a block. [8+8]

FIRSTRANKER

Code No: 07A50403

R07**Set No. 4****III B.Tech I Semester Examinations, November 2010****DIGITAL IC APPLICATIONS****Electronics And Communication Engineering****Time: 3 hours****Max Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. (a) Construct a full adder circuit using two half adders and basic logic gates.
 (b) Draw the circuit diagram of a 4-bit ripple carry adder using 4 full adder circuit blocks.
 (c) Compare and contrast ripple carry adder and a carry-look-ahead adder for same number of input bits. [6+5+5]
2. (a) Describe how floating point numbers are declared in VHDL code as per IEEE standard specifications.
 (b) Discuss the conditions under which, floating-point numbers can be subtracted or added.
 (c) Write a VHDL code to compare two 2-bit vectors to verify whether vectors are same or not. [6+5+5]
3. With the help of internal structure of a small SRAM and its timing diagram, describe Read and write operations performed in the SRAM. [16]
4. Draw the typical Input-Output transfer characteristics of CMOS Inverter and explain about the various terms associated with the characteristics. Explain the term Noise Margin. [16]
5. Explain briefly about the following statements:
 (a) Signal assignment statement
 (b) Conditional signal assignment statement
 (c) Select signal assignment statement
 (d) Variable assignment statement. [16]
6. (a) Discuss how clock skew affects the reliability of a synchronous system.
 (b) Describe synchronous system structures, which enable completion of control and data-transfer operations of a synchronous system within one cycle of clock.
 (c) Write a VHDL program to simulate the behavior of a synchronous down counter similar to 74x163. [6+5+5]
7. Explain how CMOS-TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same. [16]
8. What are the different register types in VHDL? Explain about each of them giving examples. [16]

Code No: 07A50403

R07

Set No. 4

FIRSTRANKER

Code No: 07A50403

R07**Set No. 1****III B.Tech I Semester Examinations, November 2010****DIGITAL IC APPLICATIONS****Electronics And Communication Engineering****Time: 3 hours****Max Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. (a) Draw the timing diagram to specify typical timing parameters of an SRAM to perform write operation.
- (b) Describe the sequence of operations taking place in a DRAM cell to refresh the cell after write operation is performed. [16]
2. Write structural VHDL program for 5-bit prime number detector. [16]
3. What are the different types of operators pertaining to VHDL? Explain about them. [16]
4. Describe the best practices for eliminating clock gating and clock-skew related problems in synchronous system designs. Justify the requirement of such practices. [16]
5. An odd parity circuit with $2n$ inputs can be built with $2n-1$ XOR gates. Describe two different structures for this circuit, one of which gives a minimum worst-case input-output propagation delay and the other which gives a maximum. For each structure, state the worst-case number of XOR gate delays and describe the criteria for preference of any structure. [16]
6. Write VHDL program to add two n -bit, bit-vectors and a carry and to return an n -bit sum and a carry. Give explanation. [16]
7. Draw the circuit for Diode logic AND gate and explain its operation with the help of truth table. compare this logic family with TTL and CMOS logic family. [16]
8. (a) What are the salient features of CMOS logic family. Compare this with PMOS and NMOS logic families.
- (b) Draw the circuit for CMOS NOR logic gate and explain its functioning clearly giving truth table. [8+8]

Code No: 07A50403

R07**Set No. 3****III B.Tech I Semester Examinations, November 2010****DIGITAL IC APPLICATIONS****Electronics And Communication Engineering****Time: 3 hours****Max Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. (a) Draw the circuit diagram, function table and logic symbol of an edge triggered J-K flip-flop. Explain the operation through its functional diagram.
(b) Write a VHDL code to simulate the functionality of an edge triggered J-K flip-flop. [8+8]
2. (a) Describe the sequence of operations taking place in a DRAM cell to refresh the cell after write operation is performed.
(b) Does the ROM realization remain the same even if two of the input columns are interchanged? Justify your answer. [8+8]
3. Pertaining to VHDL, using schematics explain about Multiple processes and postponed processes. [16]
4. (a) Discuss the necessity and advantages of representing integers/numbers in double precision floating-point format for arithmetic operations in digital design.
(b) Describe the steps involved in converting an integer with a range of ± 127 represented in floating point format into corresponding binary format. Explain through an example.
(c) Translate the conversion steps above into a suitable VHDL code. [6+5+5]
5. Explain about ECL 100K family and positive ECL (PECL), bringing out, salient features of the same. [16]
6. Draw the circuit for CMOS OR logic gate and explain its working clearly, giving truth table and symbol. [16]
7. What are the main statements in structural, Data flow and behavioral design elements? Explain. [16]
8. Write the VHDL code for simulating an 8x8 combinational multiplier in behavioral model explaining the steps of multiplication as comments in the code. [16]
