Code No: 07A50504 | **R07** | **Set No. 2**

III B.Tech I Semester Examinations,November 2010
MICROPROCESSORS AND INTERFACING
Common to Information Technology, Instrumentation And Control
Engineering, Electronics And Computer Engineering, Computer Science
And Engineering

Time: 3 hours
Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Explain the Interrupts of 80286 in the order of priority?

   (b) Explain the salient features of Pentium Processor? [8+8]

2. (a) Explain memory addressing modes of 8086? Give an example for each addressing mode?

   (b) What is the purpose of Trap flag? Discuss how debugging feature is provided with the help of Trap flag in 8086? [8+8]

3. Describe the function of the following pins in 8086 maximum mode of operation.

   (a) MN/ $\overline{MX}$

   (b) RQ/GT$_0$ and RQ/GT$_1$

   (c) QS$_0$ & QS$_1$

   (d) $\overline{LOCK}$ [16]

4. (a) Using REPEAT-UNTIL construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again.

   (b) What is a procedure? Give an example to declare a procedure as near? Make this procedure as PUBLIC procedure? [8+8]

5. (a) Explain the application of stepper motor in microcomputers?

   (b) Explain with a neat block diagram the working of dual slope ADC? How do you interface the dual slope ADC to microprocessor? Give the required instruction sequence to acquire one sample from ADC? [8+8]

6. (a) Discuss the following signal descriptions?

       i. $\overline{INT_0}/\overline{INT_1}$
      ii. TXD
     iii. T$_0$ AND T$_1$
      iv. $\overline{RD}$

   (b) Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?

       i. TMOD

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    ii. PSW   [8+8]

7. In an 8086 based system it is necessary to serve 64 IRQs from different initiators. The allocated address space for 8259s is from 0700h to 070FH. Give the complete design by choosing the appropriate address locations in the above range? Give the initialization sequence for all 8259's with each IRQ activated in level triggered mode and the starting interrupt is type 40H? [16]

8. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?

   (b) Interface 8251 with 8086 at address 0F0H. Initialize it in asynchronous mode, with 8 bit character size, baud rate factor 16, one start bit, two stop bits, even parity enable? [8+8]

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Code No: 07A50504   **R07**   **Set No. 4**

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1. (a) Draw the block diagram of 8086 and explain each block.

   (b) Discuss the addressing modes provided by 8086 and explain with examples.
   [8+8]

2. (a) Using DF flag and string instructions, write an assembly language program to move a block of data of length 'N from source to destination. Assume all possible conditions.

   (b) Discuss how procedures are defined and involved in assembly language programming.
   [8+8]

3. Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority? [16]

4. (a) Explain USB operation?

   (b) Interface 8251 with 8086 at address 0A010H. Initialize it in asynchronous mode, with 6 bit character size, baud rate factor 16, one start bit, two stop bits, odd parity enable? [8+8]

5. (a) Explain DOS interrupt 21H and its functions?

   (b) Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 interrupt? [8+8]

6. It is necessary to initialize interrupt for mode 2 operation of port-A and mode 1 operation of port-B with the 8255 address map of 0600H to 0603H. Give the complete hard ware design to interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A and Port B to mode 1? [16]

7. (a) Explain the paging system of 80386.

   (b) Explain the protected virtual address mode of 80286 and show how 24 bit physical address is generated. [8+8]

8. Interface two 8255s to 8051 with starting address of 0FFF0H? Show the hardware design? Write the instruction sequence to initialize all ports of 8255s as input ports in mode 0. [16]

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Code No: 07A50504 | R07 | Set No. 4

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FIRSTRANKER

4

Code No: 07A50504 **R07** **Set No. 1**

III B.Tech I Semester Examinations,November 2010
MICROPROCESSORS AND INTERFACING
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Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
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1. (a) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two-digit Hex number?

   (b) Give the assembly language implementation of the following.

      i. REPEAT - UNTIL
      ii. FOR   [8+8]

2. (a) Explain initialization command words and their sequence of operation?

   (b) Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 interrupt?   [8+8]

3. (a) How do we connect RS-232C equipment

      i. To data terminal type devices?
      ii. To serial port of SDK 86, RS-232C connection?

   (b) Give the specifications of

      i. RS-232C
      ii. RS-423A   [8+8]

4. Discuss the following signal descriptions?

   (a) ALE/PROG

   (b) $\overline{EA}$ / V_{PP}

   (c) $\overline{PSEN}$

   (d) RXD

   (e) $\overline{INT_0}$ / $\overline{INT_1}$

   (f) TXD

   (g) T_0 AND T_1

   (h) $\overline{RD}$ [16]

5. 8086 processor do not provide memory indirect addressing mode. Show all possible ways to access a word from memory where the segment address is given in location C000H:1000H and the offset is given in location C000H:1002H. Give the instruction sequence for every addressing mode of 8086.?   [16]

6. (a) How many local and global descriptors can be defined in 80286 and explain how to access them?

   (b) Discuss the branch prediction logic of Pentium processor? [8+8]

7. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait status and draw the corresponding timing diagram. [16]

8. Interface an 8-bit DAC to 8255 with an address map of 0804H to 0807H. The DAC provides output in the range of +5V to - 5V. Write the instruction sequence for the following?

   (a) For generating a square wave with a peak to peak voltage of 2V and the frequency will be selected from memory location 'FREQ'.

   (b) For generating a triangular wave with a maximum voltage of +4V and a minimum of -2V. [8+8]

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Code No: 07A50504 **R07** **Set No. 3**

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Answer any FIVE Questions
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1. (a) Write a sequence of instructions to communicate to a modem using 8251 at address 080H.

   (b) Give the specifications of

      i. RS-232C

      ii. RS-423A [8+8]

2. (a) What is the purpose of operational command words of 8259? Explain their format and the use.

   (b) Explain the following terms with reference to 8259.

      i. Fully nested mode

      ii. Automatic rotation [8+8]

3. Describe the function of the following pins and their use in 8086 based system.

   (a) NMI

   (b) $\overline{LOCK}$

   (c) $\overline{TEST}$

   (d) RESET [16]

4. (a) Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?

   (b) Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again. [8+8]

5. (a) Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?

      i. SCON

      ii. TCON

   (b) Discuss the following signal descriptions?

      i. ALE/PROG

      ii. $\overline{EA}$ / V_{pp}

      iii. $\overline{PSEN}$

7

    iv. RXD   [8+8]

6. It is necessary to check weather the word stored in location 6000H:6000H is zero or not. Show all possible ways of testing the above condition using different addressing modes and store 0FFH if the condition is satisfied in location A000H:1002H. Otherwise store 00H.   [16]

7. (a) Discuss memory management of virtual 8086 mode in 80386.

  (b) Bring out the architectural differences between 80386 and Pentium processors.
           [8+8]

8. Interface a stepper motor with 8-step input sequence to 8086 based system and write the instruction sequence to move the stepper motor 20 steps in clockwise and 12 steps in anti-clockwise direction.   [16]

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