Code No: 07A51403 **R07** **Set No. 2**

III B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive a logic circuit for a four bit parity checks using even parity
   (b) Design a 5 to 32 lines decoder using 3 to 8 and 2 to 4 decodes units. [8+8]

2. Realize the following four Boolean functions using PAL.
   (a) $F_1(w,x,y,z) = \sum(0,1,2,3,7,9,11)$
   (b) $F_2(w,x,y,z) = \sum(0,1,2,3,10,12,14)$
   (c) $F_3(w,x,y,z) = \sum(0,1,2,3,10,13,15)$
   (d) $F_4(w,x,y,z) = \sum(4,5,6,7,9,15)$ [16]

3. (a) Determine if the following boolean equation is valid or not.
   $\bar{x}_1\bar{x}_3 + x_2x_3 + x_1\bar{x}_2 = \bar{x}_1x_2 + x_1x_3 + \bar{x}_2\bar{x}_3$
   (b) Derive the simplest product of sum expression for
   $f = (\bar{x}_1 + x_2 + x_3)(\bar{x}_1 + \bar{x}_2 + \bar{x}_4)(\bar{x}_1 + x_3 + x_4)$ [8+8]

4. Design a clocked sequential circuit to detect 1111 or 0000 and produce an output Z = 1 at the end of the sequence. Overlapping is allowed. Draw the circuit using D-flip flops. [16]

5. For the machine shown in table
   (a) Obtain the corresponding reduced machine table in standard form.
   (b) Find a minimum length that distinguishes State A from State B. [8+8]

	NS, Z	
PS	X = 0	X = 1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

6. (a) Implement the logic shown below figure 1 using NAND gates only

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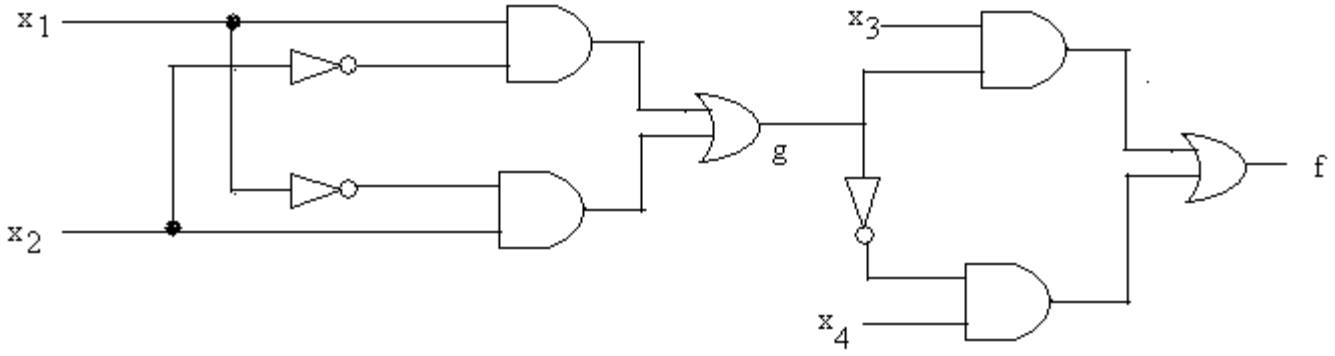

Figure 1:

(b) Find the simplest realization of the function given below, assuming that the logic gates have a maximum fan-in of two $f(x_1, x_2, x_3, x_4) = \sum M(0, 4, 8, 13, 14, 15)$ [8+8]

7. (a) Explain the Mealy state diagram and draw the ASM chart for it.
   (b) Construct the ASM chart for SR flip flop. [8+8]

8. (a) By writing parity code (even) and three times repitition code for all possible 4 bit straight binary numbers, Prove that the Hamming distance in the 2 cases is atleast 2.
   (b) Distinguish between weighted and unweighted codes. Give two examples each of both types of codes. [8+8]

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1. (a) Design a code converter which converts 8421 code to 641-1 code realize the circuit using logic gates.
   (b) Use Tabular method and minimize $f = \Pi\,(0, 3, 7, 9, 11, 12, 14)$ [8+8]

2. (a) Define the terms
      i. Cyclic codes
      ii. Reflective code
      iii. Unit distance codes
      Also show that Gray code is both reflective and unit distance code
   (b) Convert $(A98B)_{12}$ to $(\ \ )_3$
   (c) Write down the decimal code 6,3,1,-1 and prove that it is self complementing BCD codes. [6+5+5]

3. (a) Draw the ASM chart for the following state transition, start from the initial state T_1,then if xy = 00 go to T_2, if xy =01 go to T_3, if xy = 10 go to T_1, other wise go to T_3.
   (b) Prove that the multiplication of two n-bit numbers gives a product of length less than or equal to 2n bits [8+8]

4. (a) Obtain the logic function $f(x_1,x_2,x_3,x_4)$ realized by the threshold network shown in figure 2.

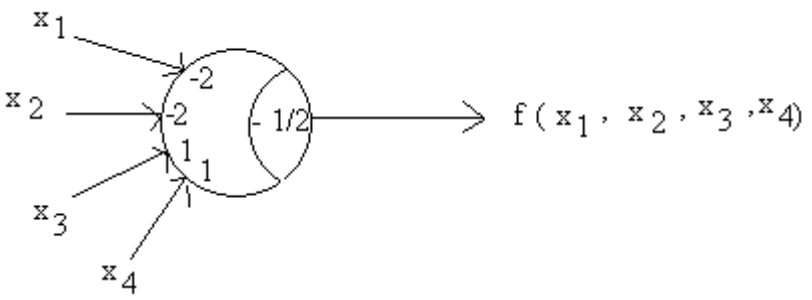

Figure 2:

   (b) Find whether the function F(w,x,y,z) $=\sum(0,1,3,5,8,10,11,12,13,15)$ is Symmetric, and if so express the function in Symmetric notation . [8+8]

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5. (a) Show that $f(A, B, C) = \bar{A}BC + A\bar{B} + \bar{B}\bar{C}$ is a universal operation.
   (b) Find the canonical product of sums form for the functioon $f(x, y, z) = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}yz + xyz + x\bar{y}z + x\bar{y}\bar{z}$. [8+8]

6. Design and implement a 4-bit comparator using logic gates. [16

7. (a) Design a 3 input square genertor circuit suing logic gates.
   (b) Realize the following function using 16 : 1 MUXS and any other logic gates. f(A, B, C, D, E, F) = Σm(0, 1, 2, 3, 7, 8, 9, 10, 11, 15, 32, 33, 34, 35, 39, 40, 41, 42, 43, 45, 47) [8+8]

8. (a) Find the maximum compatibles for the machines given below.
   (b) Show the compatibles (BD) and (CD) can be 'deleted'. Find the set of symbolic compatibles and a minimal closed cover for the machine. [16]

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PS	NS, Z			
	11	12	13	14
A	-,-	B,-	-,-	-,1
B	A,-	-,-	C,0	-,-
C	-,-	-,-	-,-	D,1
D	B,-	A,-	B,-	F,0
E	C,-	C,-	A,-	-,0
F	-,0	B,-	-,-	H1
G	-,1	F,1	E,1	D1
H	-,1	G,-	-,-	E,-

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1. (a) Implement a 4 to 1 digital MUX using a decode and 4 tristate buffers.
   (b) What is the difference between encode and digital multiplexes?
   (c) Give 4 applications of a decode. [16]

2. (a) Use tabulation procedure to generate the set of prime implicants and to obtain all minterm expression for
   $f = \sum(0, 1, 4, 5, 6, 7, 9, 11, 15) + \phi \sum(10, 14)$
   (b) Prove that if x and y are switching variables, then
      i. $x + y = x \oplus y \oplus xy$
      ii. $\bar{x} = x \oplus 1$ [8+8]

3. (a) Simplify $A.C + A.(C + B) + C.(C + B)$ using Boolean rules, and draw the simplest possible logic ciruit.
   (b) Prove that $F = \bar{A}.B + A.\bar{B} + A.B$ is equal to NAND operation.
   (c) Simplify the following expression
   $f = \overline{(AB + \bar{B}C)\,(B\bar{C} + \bar{A}B)}$ [5+5+6]

4. (a) Explain the limitations of finite state machines.
   (b) Find the equivalence partition and a corresponding reduced machine.

	NS, Z	
PS	X = 0	X = 1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

[16]

5. Derive a PLA programming table for the circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number. [16]

6. (a) Draw the circuit diagram of a 4-bit ring counter using D-flip flops and explain its operation with the help of bit pattern.
   (b) Find the valid states of Mod-8 shift counter with four flip flops and give the correct sequence. [8+8]

7. (a) Define the following terms:
   i. Self complementing code and give examples
   ii. Cyclic code with example.
   (b) Explain the procedure of generating the Hamming code what is the range of check bits? [10+6]

8. (a) Prove that the multiplication of two n-bit numbers gives a product of length less than or equal to 2n bits.
   (b) Explain about ASM chart [8+8]

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Code No: 07A51403 **R07** **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) While every maximal compatible is prime compatible, every machine may not be a symbolic compatible. Justify this statement. In the given below, show at least one machine which in not a symbolic compatible.
   (b) Reduce the machine given below. [8+8]

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PS	NS, Z			
	11	12	13	14
A	B,0	-,-	B,0	-,-
B	A,-	C,1	B,-	-,-
C	-,-	B,0	-,1	D,0
D	E,0	-,-	F,1	B,-
E	E,0	-,-	A,-	B,1
F	-,-	C,1	-,0	C1

2. (a) Find the complement of $f = A + \left[\left(B + \bar{C}\right).D + \bar{E}\right]F$.
   (b) Prove the following
   i. $L.\left(M + \bar{N}\right) + \bar{L}.\bar{P}.Q = \left(L + \bar{P} + Q\right).\left(\bar{L} + M + \bar{N}\right)$
   ii. $\left[A.\bar{B} + \bar{C} + \bar{D}\right].\left[D + \left(E + \bar{F}\right).G\right] = D.\left(A.\bar{B} + \bar{C}\right) + \bar{D}.G.\left(E + \bar{F}\right)$. [8+8]

3. (a) Find all the static hazards in this circuit shown below in figure 3. Changing only the parameters of the thereshold element, redesign the circuit so that all static hazards are eliminated.
   (b) Design a combinational circuit of 2 bit multipler. [8+8]

4. (a) Simplify the Boolean function given by
   $f = (A + B + C)\left(\bar{A} + B + \bar{C}\right)\left(A + \bar{B} + C\right)$, for the dont care condition expressed as $\left(\bar{A} + \bar{B}\right)\left(\bar{A} + B + C\right)$
   (b) Given a network below figure 4, determine f_3 and f_2 if $f_1 = x\bar{z} + \bar{x}z$ and the overall function f is
   $f\left(w, x, y, z\right) = \sum\left(0, 4, 9, 10, 11, 12\right)$ [8+8]

5. (a) The state of a 12bit register is 100010010111. What is its content if it represents three decimal digits in BCD, three decimal digits in Excess-3 code, three decimal digits in the 8,4, -2,-1 code
   (b) How many parity check bits required to be included with the data word to achieve single error correction and double error detection when the data word contains

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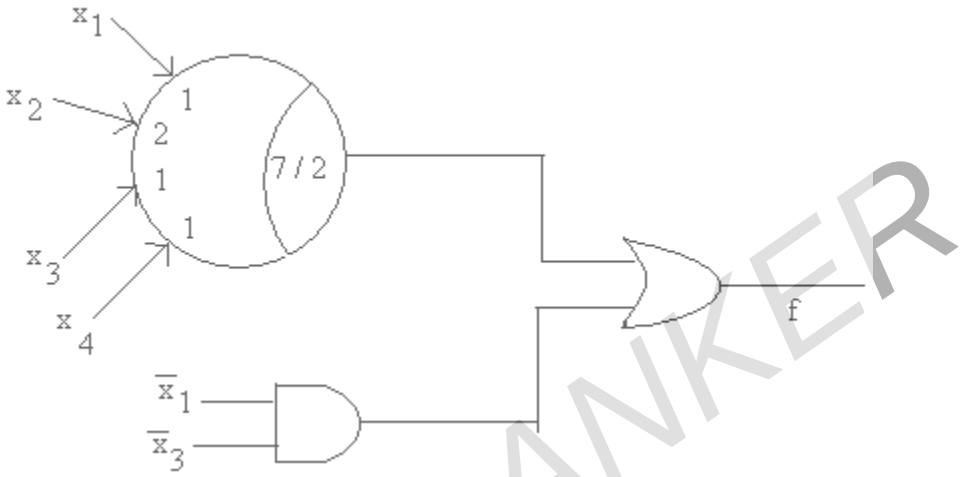

Figure 3:

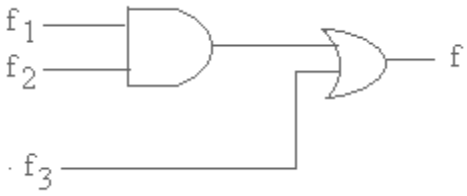

Figure 4:

i. 16 bit
ii. 32 bit
iii. 48 bit [10+6]

6. Implement the following functions using PROM.
   (a) $F_1(w,x,y,z) = \sum(0,1,7,9,12,15)$
   (b) $F_2(w,x,y,z) = \sum(0,1,2,3,4,7,8,10,12,14,15)$ [16]

7. (a) Draw the circuit diagram of a 4-bit Johnson Counter using D- Flip-Flop and explain its operation with the help of bit pattern.
   (b) At the junction of Four roads going North, South, East and West it is proposed to install traffic lights of Three colors- Red (R), amber(A) and Green(G) with Flexible time settings. Design an Asynchronous System . Assume that an Electronic Timer is available. [8+8]

8. (a) Design the control for the given state diagram 5 using one flip flop per state.
   (b) Design control circuit using flip flops and decoder. [8+8]

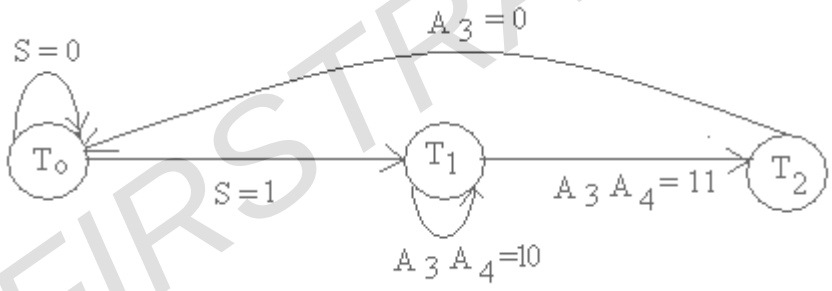

Figure 5:

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