Code No: 07A60403 **R07** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
LINEAR AND DIGITAL IC APPLICATIONS
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Classify the filters and explain the characteristics of each one of them.
   (b) Draw the first order low-pass Butterworth filter and analyze the same by deriving the gain and phase angle equation. [8+8]
2. (a) Write short notes on SDRAM. Distinguish between latch and flip-flop? Show the logic diagram for both?
   (b) Designconversion circuit to convert a D flip-flop and J-K flip-flop? [8+8]
3. (a) Derive closed loop voltage gain, input resistance, output resistance and bandwidth for inverting amplifier with feedback arrangement.
   (b) Explain any one of the frequency compensation technique in connection with Op-amp. [8+8]
4. (a) Explain the operation of Astable multivibrator using 555 timer.
   (b) Design a Monostable multivibrator using 555 timer to produce a pulse width of 200 ms. [10+6]
5. (a) With the help of logic diagram explain 74×157 multiplexer?
   (b) Design a serial binary adder? [8+8]
6. (a) Compare different logic families and mention their advantages and disadvantages?
   (b) Which is the fastest non-saturated logic gate? Draw the circuit and explain its functions. [8+8]
7. (a) Sketch and explain the transfer characteristic of a DAC with necessary equations.
   (b) LSB of a 9-bit DAC is represented by 19.6 m Volts. If an input of 9 zero bits is represented by 0 volts.
      i. Find the output of the DAC for an input, 10110 1101 and 01101 1011.
      ii. What is the Full scale Reading (FSR) of this DAC? [8+8]
8. (a) With the help of neat block diagram, explain the operation of a fixed voltage regulator.
   (b) Describe the operation of an IC based negative voltage regulator. Give few applications.

(c) Describe the principle of operation of a peak detector with wave forms.[6+6+4]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A60403 **R07** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
LINEAR AND DIGITAL IC APPLICATIONS
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the basic circuit diagram of an Op-amp and explain the operation of each block.
   (b) Write detailed notes on any four applications of Op-amp. [8+8]
2. (a) Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics?
   (b) Explain the following terms with reference to TTL gate?
      i. Logic levels.
      ii. DC Noise margin.
      iii. Low-state unit load.
      iv. High-state fan out. [8+8]
3. Write short notes on the operation of any two:
   (a) Quadrature oscillator.
   (b) Voltage controlled oscillator.
   (c) Wien - bridge oscillator. [16]
4. (a) Explain the operation of an 8-bit tracking type Analog to Digital converter.
   (b) Compare the conversion times and efficiencies of 8-bit tracking type and successive approximation type Analog to Digital converters. [8+8]
5. (a) What is the necessity of tri state buffer?
   (b) Design a 16-bit comparator using 74×85 ICs? [8+8]
6. (a) Sketch the circuit of a logarithmic amplifier using one Op-amp and explain its operation. State its application.
   (b) What is a sample and hold circuit? Why is it needed? Draw a sample and hold circuit and explain its operation. [8+8]
7. (a) Design a 4-bit binary synchronous counter using 74×74?
   (b) Draw the circuit and explain the crystal controlled clock generators. [8+8]
8. (a) List the application of IC 565PLL and briefly describe the role of the PLL in any of that application.

(b) Referring to the circuit shown in figure 8b determine the free running output, lock range and the capture range . [8+8]

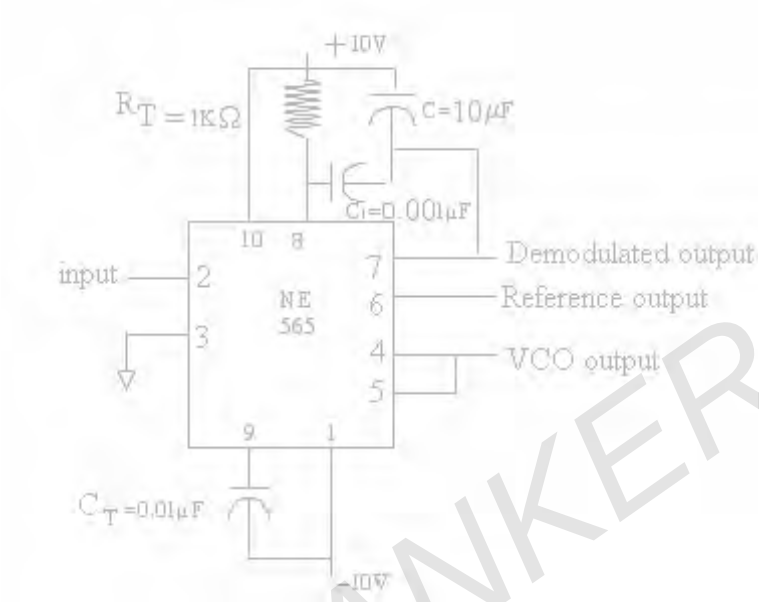

Figure 8b

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A60403 **R07** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
LINEAR AND DIGITAL IC APPLICATIONS
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What is the working principle of PLL? Explain.
   (b) Give the block diagram of PLL and explain about each block in detail.
   (c) Give any one application of PLL. [4+8+4]
2. (a) Draw the circuit of a typical instrumentation amplifier. Why do we use two stage op-amp circuit as an instrumentation amplifier. Explain?
   (b) What is the difference between a basic comparator and the Schmitt trigger? Construct a Schmitt trigger circuit using Op-amp and derive the threshold voltages. [8+8]
3. (a) Define by means of a diagram the pass band, stop band, transition band and pass band ripple.
   (b) Sketch the ideal frequency-response characteristics of Low pass, high pass and band reject filters.
   (c) Design a second order low pass filter at a higher cut off frequency of 2KHz. [5+5+6]
4. (a) Briefly explain the characteristics of an ideal Op-amp.
   (b) What do you mean by input offset voltage and input offset current of an Op-amp? Explain and give the experimental setup to measure these parameters.
   (c) For the non-inverting AC amplifier $R_{in} = 50\Omega$, $C_i = 0.1\mu f$ $R_1 = 1K\Omega$, $R_{0M} = 820\Omega$, $R_F = 5.6K\Omega$ and $R_L = 10K\Omega$. Determine the gain & band width of the amplifier (figure 4c). [3+7+6]

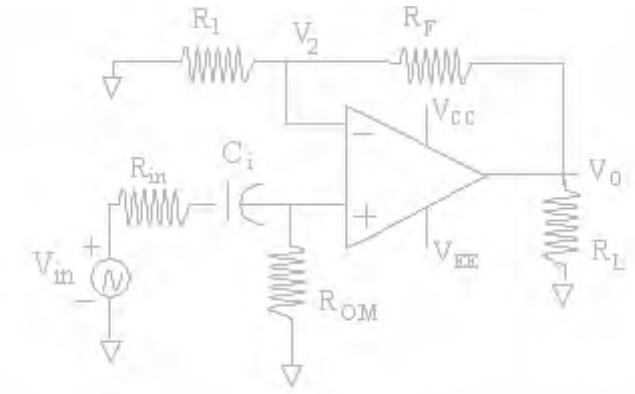

Figure 4c

5. List out standard TTL Characteristics and explain them briefly with necessary diagrams. [16]

6. (a) Explain with an example why asynchronous inputs are required in flip flops.
   (b) Explain the operation of edge triggered T flip- flop. [8+8]

7. (a) A counting type ADC uses a 8bit DAC. The MSB of DAC output voltage is +5V
      i. If the analog I/P voltage is +6.85 V, what will be the R-2R ladder o/p voltage when the clock stops?
      ii. What is the no.of clock pulses that occur between the release of reset and stopping of the clock?
   (b) Calculate the values of the LSB, MSB at full scale output for an 8 bit DAC for the 0 to 10 V range. [5+5+6]

8. (a) Give the working principle of Analog-Multiplexer. Give block diagram of a 16 input analog multiplexer using CMOS gates and explain how it works?
   (b) Design a 24-bit group ripple adder using 74×283 ICs? [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A60403 **R07** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
LINEAR AND DIGITAL IC APPLICATIONS
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation?
   (b) List out TTL families and compare them with reference to propagation delay, power consumption, speed-power product and low level input current? [8+8]
2. (a) Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage Vo.
   (b) Give the schematic circuit of an A/D converter widely used in digital voltmeters and explain its operation. Derive expression for output voltage. [8+8]
3. (a) Design a 4-bit carry look ahead adder using gates.
   (b) Write short notes on BCD to gray code converter. [8+8]
4. (a) What are the two basic modes in which the 555 timer operates? Briefly explain the differences between the two operating modes of the 555 timer.
   (b) Design a ramp generator using 555 timer having an output frequency of approximately 5 KHz. [8+8]
5. (a) A fourth order Butterworth polynomial is given as (S^2+0.765S+1) (S^2 + 1.848S+1). Design the fourth order Butterworth filter having upper cutoff frequency 2 KHz. Assume suitable data. Draw the circuit diagram with suitable values.
   (b) What are the gain constraints imposed on higher order filters? Explain.[10+6]
6. (a) Write short notes on synchronous up counter.
   (b) Explain the operation of Synchronous SRAM with the help of its internal Architecture. [8+8]
7. (a) Define common mode rejection ratio (CMRR)? Explain why CMRR $\rightarrow \infty$ for an emitter coupled differential amplifier where $R_E \rightarrow \infty$.
   (b) Why is cascade configuration used in an Op-amp?
   (c) Explain with the figures how two supply voltages $V^+$and V^- are obtained from a single supply. [8+4+4]
8. (a) Draw the circuit diagram of an inverting amplifier and obtain the expression for it's output voltage..

(b) For the ciruict shown in figure 8b

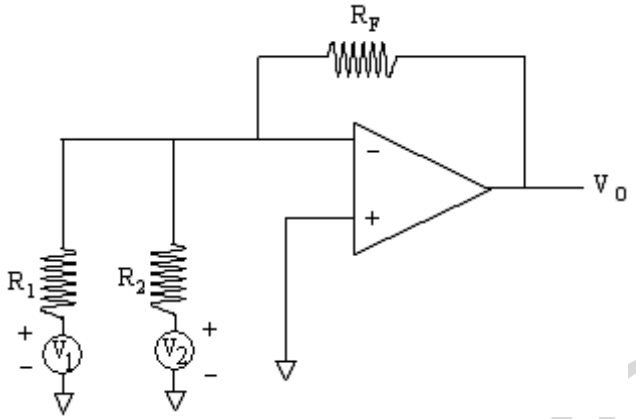

Figure 8b

Find

i. Find V_0 in the above circuit if $R_f = 10$ kΩ, $R_1 = 2$ kΩ and $R_2 = 5$ kΩ.

ii. Find R_1 and R_2 if Vo is the average of V_1 and V_2 and $R_f = 10$ kΩ. Assume necessary data. [8+4+4]

⋆ ⋆ ⋆ ⋆ ⋆