Code No: 07A6EC03 **R07** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to BME, ETM, E.CONT.E, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What is the principle of FPGAs? Explain about the architectures fo FPGAs.
   (b) What are the applications of FPGAs? Explain. [8+8]
2. Draw the circuit for NMOS Inverter and explain its operation. [16]
3. (a) Explain the processing steps in fabrication of nmos technology with neat sketches.
   (b) Explain any one method of encapsulation of IC. [10+6]
4. Write notes on any TWO
   (a) DGT
   (b) BIST
   (c) Boundary scan Testing. [8×2=16]
5. (a) What is meant by Timning simulation with suitable example in VLSI Design? Explain.
   (b) Explain about Flattening and Factoring in VHDL simulation. [8+8]
6. Give the topology for four bit carry select module and explain its operation in detail. [16]
7. (a) Design a complimentary static CMOS XOR gate. Explain the steps involved and draw the logic circuit.
   (b) What are the issues involved in driving large capacitor loads in VLSI circuit designs? Eaxplain. [8+8]
8. (a) Explain about the effect of scaling on MOSFET parameters.
      i. Gate Area
      ii. Gate capacitance
      iii. Channel Resistance
      iv. Transistor Delay
   (b) Explain about Design Rules for contact cuts. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A6EC03 **R07** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to BME, ETM, E.CONT.E, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the circuit and layout schematic for 2-input NOR gate giving explanation.
   (b) What are the various limitations of scaling? [8+8]
2. Draw the circuit for CMOS inverter and explain the transfer characteristic using necessary equations, and the different regions in the characteristic. [16]
3. (a) Explain about Event-Driven simulation.
   (b) What is meant by Logic synthesis? Explain. [8+8]
4. (a) Give a schematic for memeory self-test and explain the same.
   (b) What are the advantages of implementing BIST? Explain. [10+6]
5. What are the circuit design considerations in the case of static adder circuits? [16]
6. (a) With the help of sketches explain the principles of different types of diffusion' Processes.
   (b) Explain about Fick's laws of diffusion. [10+6]
7. (a) Explain the structure and principle of PLA.
   (b) Draw the schematic and explain how Full Adder can be implemented using PLA's. [6+10]
8. (a) Explain the concept of sheet resistance and sheet capacitance. Give examples.
   (b) What are the design issues involved in long interconnect wires? Explain.[8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A6EC03 **R07** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to BME, ETM, E.CONT.E, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain the processing steps in fabrication of PMOS technology with neat sketches.
   (b) What are the additional two layers in BICMOS technology compared to other. [10+6]
2. (a) Explain about stick diagram.
   (b) Explain about scaling. [8+8]
3. (a) Draw the circuit of CMOS Inverter and explain its operation.
   (b) What are the various pull up transistor used for inverters? [8+8]
4. (a) What are the issues involved in driving large capacitive loads in VLSI circuits? Explain.
   (b) Derive the expression for τ_{SD} in the case of a MOSFET. [8+8]
5. (a) With the help of a schematic explain about Memory-self Test.
   (b) What are the issues to be considered while implementing BIST? Explain. [8+8]
6. Draw the schematic for Wallace Tree for four bit Multiplier and explain its operation. [16]
7. (a) Write a code in VHDL for a serial-in/parallel-out(SIPO) shift register.
   (b) Explain how addition can be carried out using a ripple-carry architecture in VHDL. Write the code for the same. [8+8]
8. (a) Draw the structure of programmable Array logic(PAL) and explain its principle of operation.
   (b) Explain about different methods of implementation approaches in VLSI Design. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A6EC03 **R07** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to BME, ETM, E.CONT.E, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Explain the principle and working of CPLDs and give their applications. [16]
2. (a) With the help of a flow chart explain the method of Testing at various stages in VLSI Design cycle.
   (b) Why testing is needed in VLSI design? Explain the principle of testing. [8+8]
3. Draw the circuits for n-MOS, p-MOS and C-MOS Inverter and explain about their operation and compare them. [16]
4. (a) Explain about bit sliced Data path organization. What is the significance of Data paths in digital processors?
   (b) Give the Truth Table for full adder and explain its Boolean expression. [8+8]
5. (a) What are the different types of oxidation processes? Explain.
   (b) With the help of neat sketches, explain the steps involved in photolithography and pattern transfer. [8+8]
6. (a) What are the various constraints in Synthesis Process? Explain.
   (b) Using block schematics, explain about attributes in synthesis process. [8+8]
7. Explain about Static Logic, Dynamic Logic and Domino Logic and compare them in all respects. [16]
8. (a) Why scaling is required?
   (b) How does Depletion Regions around Source and Drain are affected due to scaling down of device dimensions? Explain. [6+10]

⋆ ⋆ ⋆ ⋆ ⋆