Code No: 07A6EC14 **R07** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the following
   i. Microoperation
   ii. Microinstruction
   iii. Microprogram
   iv. Control memory
   (b) What is meant by writable control memory and explain microprogram control organisation. [8+8]
2. (a) What is the Flynn's classification of computer system and explain.
   (b) What is pipeline? Explain the concept of instruction pipeline. What are its advantages? [8+8]
3. Write about performance measure of a computer. [16]
4. Differentiate between serial arbitration and parallel arbitration . [16]
5. In a paging system the virtual address contains 8K sizes pages with the bit configuration as 1010011001101 the corresponding page table entry for the page number is 11, what is the contents of the main memory address [16]
6. (a) Obtain the truth table of an 8 ×3 priority encoder. Assume that the three outputs xyz from the priority encoder are used to provide a vector address of the form 1010xyz00. List the eight vector addresses starting from the one with the highest priority.
   (b) Show how zero insertion works in the bit-oriented protocol when a zero followed by the 10 bits that represent the binary equivalent of 1023 are transmitted. [8+8]
7. A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other three addresses if the addressing mode of the instruction is
   (a) Direct
   (b) Indirect
   (c) Relative

(d) Indexed. [4+4+4+4]

8. (a) Explain the operation of BCD adder/subtractor.
   (b) Explain decimal division algorithm. [8+8]

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COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the following
   i. Microoperation
   ii. Microinstruction
   iii. Microprogram
   iv. Control memory
   (b) Differentiate between Hardwired control and microprogrammed control. [8+8]
2. Write the following techniques in dynamic arbitration algorithm
   (a) Time slice
   (b) rotating daisy chain
   (c) LRU
   (d) FIFO. [4×4]
3. What is Asynchronous Data Transfer? Explain various methods of asynchronous data transfer with timing diagrams. [16]
4. Discuss the following with examples.
   (a) Zero-address instructions
   (b) One-address instructions
   (c) Two-address instructions
   (d) Three-address instructions. [4+4+4+4]
5. (a) Write about instruction format for vector processor.
   (b) Explain the concept of pipeline in calculating inner product. [8+8]
6. (a) Describe a magnetic tape drive and its controller.
   (b) A Computer needs 2K bytes of RAM and 4K bytes of ROM. How many RAM chips and ROM chips are needed if there are only 128x8 RAM chips and 512x8 ROM chips are available? [8+8]
7. (a) Give the 2's complement notation for the following signed decimal numbers for 8-bit word:
   i. +1
   ii. +127

iii. -1
iv. -128

(b) Obtain the 1's and 2's complement of the following
i. 10101110
ii. 10000001
iii. 10000000
iv. 000000.01 [8+8]

8. (a) Explain the operation of BCD adder/subtractor.
(b) Design an array multiplier that multiples two 4-bit numbers. Use AND gates and binary adders. [8+8]

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Code No: 07A6EC14 **R07** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Draw the flowchart for 4-segment pipeline and explain each step in it.
   (b) What do you mean by pipeline conflicts? Explain with an example. [8+8]
2. (a) What is meant by virtual memory? Explain different virtual memory techniques.
   (b) What is paging explain how the techniques of paging can be implemented. [8+8]
3. (a) Explain the execution of subroutine call and return operations using microoperations.
   (b) Explain the interrupt handling mechanism in a computer. [8+8]
4. (a) Discuss in detail the design of control unit.
   (b) How do you map micro operation to a micro instruction address. [8+8]
5. Write about the following
   (a) system bus
   (b) synchronous bus
   (c) asynchronous bus. [6+6+5]
6. (a) List the 10 BCD digits with an even parity in the left most position (total five digits per bit) Repeat with an odd parity bit.
   (b) Perform the arithmetic operations (+42) + (-13) and (-42) (-13) in binary using signed 2's complement representation for negative numbers. [8+8]
7. (a) Derive an algorithm in flowchart form for nonrestoring method of fixed- point binary division.
   (b) Explain decimal division algorithm.Design an array multiplier that multiples two 4-bit numbers. Use AND gates and binary adders. [8+8]
8. (a) Explain the asynchronous data transfer schemes.
   (b) What is an interrupt? Explain about priority Interrupt. [8+8]

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Code No: 07A6EC14 **R07** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is the advantage of priority interrupt over non priority interrupt? Explain the use of mask register?
   (b) Write the important flag conditions checked by the processor during programmed I/O? [8+8]
2. (a) What is system software? List various functions of it.
   (b) Compare Multiprocessors and multicomputers. [8+8]
3. The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words in each. Physical memory consists of 4K blocks of 4K words in each. Formulate the logical and physical address formats. [16]
4. (a) What is a bus? And construct a bus system using multiplexers.
   (b) List and explain Arithmetic microoperations. [8+8]
5. (a) Explain about symbolic Microinstructions.
   (b) Why do we need some bits of current microinstruction to generate address of the next microinstruction. Support with an example. [8+8]
6. (a) Write about dynamic arbitration algorithms
   (b) Explain the Daisy chain arbitration. [8+8]
7. (a) Consider the decimal numbers 575 and -320, find their sum using BCD adder. Explain the stepwise operation.
   (b) Perform the arithmetic operations
      i. (+25) + (+15)
      ii. (-25) + (+35) [8+8]
8. A non pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns.Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? [16]

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