Code No: 07A7EC32 **R07** **Set No. 2**

IV B.Tech I Semester Examinations,NOVEMBER 2010
VLSI DESIGN
Common to Electronics And Computer Engineering, Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Draw the structure, explain the function and write the applications characteristics of the following programmable CMOS devices: [16]
   (a) PLA
   (b) PAL
   (c) FPGA
   (d) CPLD.
2. (a) Design a comparator using XNOR and AND gate and draw its schematic.
   (b) Design a zero/one detector and draw its schematic and also calculate its delay. [8+8]
3. (a) What are the advantages of Hardware Description Languages and Software Languages?
   (b) What are different design verification tools and explain them in brief? [8+8]
4. Compare the relative merits of three different forms of pull up for an inverter circuits. What is the best choice for realization in
   (a) nMOS technology
   (b) CMOS technology. [16]
5. Discuss the Gate logic with reference to the following:
   (a) NMOS and CMOS inverters.
   (b) NMOS- NAND and CMOS NAND gates
   (c) NMOS- NOR and CMOS- NOR gates. [4+6+6]
6. Explain the following two oxidation methods in IC fabrication.
   (a) High pressure oxidation
   (b) Plasma oxidation. [8+8]
7. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]
8. (a) What are the different ATPG algorithms? Explain them briefly with suitable example.

(b) The number of nodes in a circuit is 100 and the length of test sequence 12,000. Find number of cycles need to be simulated? [8+8]

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1. Explain
   (a) Propagation delay
   (b) Wiring capacitance. [8+8]
2. Write a syntax for the following in VHDL : [16]
   (a) if
   (b) case
   (c) when
   (d) generic
   (e) entity
   (f) architecture
   (g) configuration
   (h) library.
3. (a) What are the reasons of malfunctioning of chip? What are the different levels of testing?
   (b) Explain how a parallel scan is used for data path test.
   (c) What is mean by level sensitive of logic system? [6+6+4]
4. Explain the following terms related to the fabrication of IC
   (a) Diffusion
   (b) oxidation
   (c) Lithography
   (d) Metallization. [4+4+4+4]
5. Explain the following
   (a) Double metal MOS process rules.
   (b) Design rules for P- well CMOS process. [8+8]
6. (a) What are the differences between a gate array chip and standard-cell chip? What benefits does each implementation style have?

(b) Write the equations for a full adder in SOP form. Sketch a 3-input, 2- output PLA implementing this logic. [8+8]

7. (a) Draw the serial multiplier and explain how the successive addition algorithm is implemented in it.

   (b) Design a gray-coded counter in which only one bit changes on each cycle. [8+8]

8. (a) Discuss the nFET resistance with relevant equations.

   (b) Calculate the linearized drain source resistance of an nFET with following parameters. W=8μm, L=0.5μm, k'_n=180 μA/V^2, V_{tn} =0.7V and V_{DD}=3.3V. [8+8]

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Code No: 07A7EC32 **R07** **Set No. 1**

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1. (a) What are stick diagrams?
   (b) Write stick encoding for
      i. n diffusion
      ii. Polysilicon
      iii. Metal-1
      iv. Contact cut.
   (c) Draw stick diagram for P-well CMOS inverter. [2+2+2+2+2+6]
2. (a) Explain the manufacturing test of a chip with suitable examples.
   (b) Explain how an Ad-hoc test technique used to test long counters. [8+8]
3. (a) Why resistor pull up is not used in MOS circuits?
   (b) Discuss different forms of pull up, mentioning merits and demerits of each form. [4+12]
4. (a) Write a VHDL program in behavioral modeling with concurrent signal assignment.
   (b) Explain the method of switch-level simulation for CMOS circuits and name such a simulators. [8+8]
5. (a) Compare the Antifuse and Vialink programmable interconnections for PAL devices.
   (b) What are different typically available SSI Standard-cell types and compare them. [8+8]
6. (a) Draw the logic and schematic diagrams for 4 bit ALU and explain how it performs both arithmetic and Boolean operations.
   (b) Explain how a higher radix multipliers reduce the number of adders. [8+8]
7. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [16]
8. Describe the flow diagram of Berkeley N well fabrication. [16]

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Code No: 07A7EC32 **R07** **Set No. 3**

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1. Explain the following in brief:
   (a) Chip level test techniques
   (b) System level test techniques. [8+8]
2. Mention the properties of oxidation, explaining thermal oxidation technique. [16]
3. Calculate on resistance of the circuit shown in the figure 3 from V_{DD} to GND. If n- channel sheet resistance R_{sn}=10^4 Ω per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4$ Ω per square. [16]

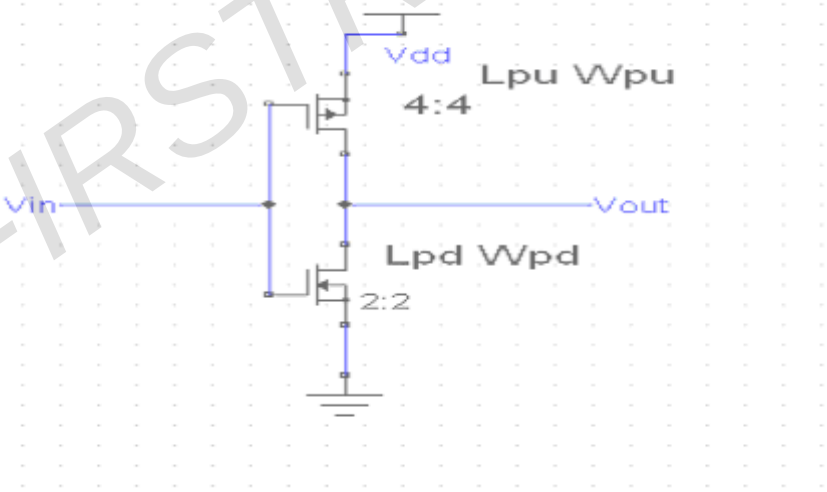

Figure 3

4. (a) Explain nMOS inverter and latch up in CMOS circuits?
   (b) Draw the nMOS transistor circuit model and explain various components of the model. [8+8]
5. Design a stick diagram and layout for the CMOS logic shown below.
   $Y = \overline{(AB) + (CD)}$ [16]
6. (a) Explain how an array is constructed to describe memories in VHDL.
   (b) Write a VHDL module which describes a 64-word x 16-bit RAM. [8+8]

7. Develop a model of word line decoder delay for a RAM with 2^n rows and 2^m columns. Assume true and complementary inputs are available and that the input capacitance equals the capacitance of one of the columns of H=2^m. Use static CMOS gates and express result in terms of n and m. [16]

8. (a) What are the characteristics of 22V10 PAL CMOS device and draw its I/O structure.

   (b) Explain any one chip architecture that used the antifuse and give its advantages. [8+8]

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