Code No: A109211002 **R09** **Set No. 2**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to Instrumentation And Control Engineering, Electronics And Computer Engineering, Electronics And Instrumentation Engineering
Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the procedure to obtain the Complement of a Function. Explain how it differs from Dual of a function.
   (b) Determine the complements of the following function.
      i. AB+ CD(AB′+CD)
      ii. AB(BC′+BC)(AC′+AB)
      iii. A + B[A +(B+C)′D]
      iv. AB + A′B′ + A′BC [8+7]
2. (a) Design a modulo-9 shift counter using T flip flops. Explain the design procedure with state diagram, state table, excitation table.
   (b) Construct a T-Latch and explain its operation. [10+5]
3. (a) i. Convert $(1596.675)_{10}$ to hexadecimal
      ii. Convert $(11110.1011)_2$ to decimal
      iii. Convert $(10110001.01101001)_2$ to octal
      iv. Convert $(235.0657)_8$ to Binary
   (b) Obtain the 1's complement and 2's complement of the binary numbers
      i. 1011011
      ii. 0110101
      iii. 10110
      iv. 00110 [8+7]
4. Minimize the following incompletely specified machine using Merger Table method. [15]

PS	NS,Z	
	X = 0	X = 1
A	E,0	B,0
B	F,0	A,0
C	E,-	C,0
D	F,1	D,0
E	C,1	C,0
F	D,-	B,0

5. (a) Design a logic circuit which accepts a 4 Binary input and converts it into BCD number. Draw the logic circuit with AND gates and OR gates.

(b) List down the Design procedure of combinational logic circuits. [8+7]

6. (a) Write short notes on ASM chart. Give the different boxes used in the ASM chart. Explain them with examples.

   (b) Write the salient features of ASM chart. [8+7]

7. List the PLA Programming table for OCTAL to BCD converter. Implement the function in a ROM and PLA. Compare both the design and justify which is the most economical. [15]

8. Design a circuit which takes 3 inputs A, B, C. The circuit should be designed in such a way that it has 8 outputs connected to LED. The LED should glow if its input is HIGH. The circuit should be designed in such a way that the one LED glows at a time based on the Input combinations. The outputs of the circuit should correspond to the minterms of the inputs. [15]

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Code No: A109211002 **R09** **Set No. 4**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
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Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
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1. What are the conditions for the two machines are to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form. [15]

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

2. Reduce the given function using Quine McC lusky method
F(A,B,C,D,E,F)=Σm (0,1,2,4,6,9,12,16,21,25,29,32,37,41,43,45,56,58,62,63) [15]

3. Explain the construction and working of SR flip Flop for different input conditions. Explain in detail the output conditions of SR flip flop if S=R=1.How the circuit is modified to avoid this conditions. [15]

4. (a) Prove the following identity
XY + X′Y′ +YZ = XY +X′Y′ +X′Z
   (b) Define Switching functions. Consider a 3 variable switching function and create a Truth table for all possible values of the input.
   (c) Consider 2 functions, f = x′y +xyz′ & g = xy′ + xz. For all possible values of x,y,z create a truth table for the outputs f, g, f+g and f′. [4+4+7]

5. Design a sequential logic circuit of a 4 bit counter to start counting from 0000 to 1000 and this process should go on. Draw the ASM chart and design the Data processing unit and the control unit. [15]

6. (a) Design a full adder circuit using 2 half adders.
   (b) Design a 4 bit Parallel adder using full adders. [8+7]

7. Implement the following Boolean functions using ROM and PAL.
F1(x,y,z) = Σ(0,1,5,7)
F2(x,y,z) = Σ(1,2,3,6,7)

F3(x,y,z) = Σ(3,5,6,7)
F4(x,y,z) = Σ(0,2,3,4,6) [15]

8. (a) Explain the procedure for converting Gray code to Binary code with an example.
   (b) Explain the procedure for converting Binary code to Gray code with an example. [8+7]

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Code No: A109211002 **R09** **Set No. 1**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
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Answer any FIVE Questions
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1. Draw the ASM for the following sequence.
   $0000 \rightarrow 0001 \rightarrow 0010 \rightarrow 0011 \rightarrow 0100 \rightarrow 0000$ and continues.
   Design the data processing unit and control unit to implement the above mentioned design. [15]

2. (a) Simplify using Boolean postulates and verify using K-map the following
      i. (x+y′+xy′)(xy+x′z+yz)
      ii. (A+B)(A′+C)(B+C)
   (b) Simplify the following function using K-map
   F = Π M(1,5,7,9,11,13) [11+4]

3. (a) Define Truth table with examples. Define Huntington Postulates.
   (b) Implement the following Boolean functions as logic circuits
   F1 = (AB + C′D)′(A′B xor D)′(C′D)′
   F2 = (A + B[A+(B+C)′D]′) [8+7]

4. (a) Explain how decoder acts as a demultiplexer.
   (b) Realize the logic function using 8:1 multiplexer
   F(w,x,y,z) = Σm(0,1,3,5,6,15) [8+7]

5. For the machine shown, find the equivalent partition and a corresponding reduced machine in standard form. [15]

PS	NS,Z	
	X = 0	X = 1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

6. (a) Solve for X
      i. $(F3A7C2)_{16} = (X)_{10}$
      ii. $(2AC5)_{16} = (10949)_X$
      iii. $(0.93)_{10} = (X)_8$

iv. $(4057.06)_8 = (X)_{10}$

(b) The message given below has been coded in the Hamming code and transmitted through a noisy channel. Decode the message assuming that at most a single error has occurred in each code word of 8 bits.
1 0 0 1 0 0 1 0 1 1 1 0 0 1 1 1 1 0 1 1 0 0 0 1 1 0 1 1 [8+7]

7. A combinational logic circuit is defined by the following functions.
F1(w,x,y,z) = Σ(1,3,12)
F2(w,x,y,z) = Σ(1,2,5,7,8,9,10)
F3(w,x,y,z) = Σ(0,1,2,4,6,8,9,12,15)
F4(w,x,y,z) = Σ(1,2,3,5,7,9,12,14,15)
Implement the circuit using PLA. [15]

8. A long sequence of pulses enters a 2 input, 2 output synchronous sequential circuit, which is required to produce an output pulse y =1 whenever the sequence 1010 occurs. Overlapping sequences are accepted.

(a) Draw the state diagram.

(b) Select an assignment and show the excitation and output tables.

(c) Write the excitation table for JK flip flop and draw the corresponding logic diagram. [15]

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Code No: A109211002 **R09** **Set No. 3**

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Answer any FIVE Questions
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1. (a) Differentiate Hexadecimal codes and Alpha numeric codes
   (b) Write Gray codes for the following decimal numbers
      i. 1000
      ii. 724
      iii. 83
      iv. 37

   [8+7]

2. Design a combinational logic circuit to convert the input Gray code into equivalent BCD code using a Multiplexer. Write the truth table to indicate the conversion. Draw the logic diagram. [15]

3. (a) Obtain the ASM chart for the following state transition. State T1 starts and then goes to state T2 when AB = 00, then goes to state T3 when AB = 01 and then goes to state T1 when AB = 10, otherwise to state T3.
   (b) Draw an ASM chart for a DATA flip flop. [8+7]

4. Minimize the following incompletely specified machine using Merger Graph method. [15]

PS	NS,Z			
	I1	I2	I3	I4
A	-	C,1	E,1	B,1
B	E,0	-	-	-
C	F,0	F,1	-	-
D	-	-	B,1	-
E	-	F,0	A,0	D,1
F	C,0	-	B,0	C,1

5. (a) Define the Distributive law and Idempotence law with examples
   (b) Prove that
      i. AB + A′C = (A +C)(A′+B)
      ii. (A+B) (A′+C)(B+C) = (A+B)(A′+C) [8+7]

6. (a) Design a clocked SR flip flop. Explain its operation with the help of characteristic table and characteristic equation. Give the symbol of edge triggered SR flipflop.

(b) Explain the operation of JK flipflop with the help of input output waveforms. [8+7]

7. A digital system has 4 inputs W, X,Y, Z. If any three, or all four inputs are HIGH The output F must go HIGH. If only 2 inputs are HIGH, then the output will take the value of Z. If only one, or none, of the inputs is HIGH the output must be LOW. Design the circuit. [15]

8. Design a 4 input priority encoder in a ROM and PAL. [15]

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