Code No: NR/RR 221003 | **NR/RR** | Set No. 2

II B.Tech II Semester Examinations,December 2010
PULSE AND DIGITAL CIRCUITS
Common to Electronics And Control Engineering, Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Bring out the necessity and importance of Time base circuits. [6]
   (b) In the UJT sweep circuit, V_{BB} = 20V, V_{yy} = 50V, R=5k, C=0.01 micro F. UJT has η= 0.5. Calculate
      i. amplitude of sweep signal
      ii. Slope and displacement errors and
      iii. estimated recovery time. [10]

   Design a collector coupled monostable multi to meet the following specifications:

   silicon n-p-n transistors are used in the design with h_{fe} (min)=20,V_{BE} cutoff voltage for the normally OFF transistor is -1V; I_{CBO} and voltage drops across saturated transistors are negligible. The base drive to the transistor in saturation is 60% in excess of minimum required. Vcc=9V,Ic=3mA.pulse width is 4msec.choose R_{C1}=R_{C2} and R_1=R_2. [16]

2. (a) A symmetrical square wave of peak to peak amplitude V and frequency 'f ' is applied to a high pass RC circuit. Find the percentage tilt. [12]
   (b) How can this tilt be reduced? [4]

4. (a) Calculate the output levels of the following circuit for inputs of 0 and -6 Volts and verify that the circuit is an inverter. What is the minimum value of h_{FE} required. Neglect junction saturation voltages and assume an ideal diode. (figure 2a) [8]

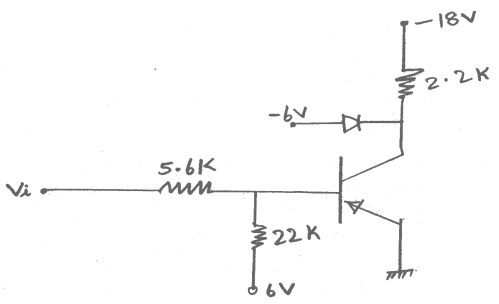

Figure 2a

   (b) Write about diode switching times. [8]

5. (a) Illustrate the terms 'synchronization' and 'frequency division' of a sweep generator. [8]

   (b) A free-running relaxation oscillator has sweep amplitude of 100 V and a period of 1 msec synchronizing pulses are applied to the device such that breakdown voltage is lowered by 50 V at each pulse. The synchronizing pulse frequency is 4 kHz. What is the amplitude and frequency of synchronized oscillator waveform? [8]

6. Explain the operation of an RC controlled free running blocking oscillator with neat sketch of circuit and voltage waveforms. Derive the expression for duty cycle. What are the advantages of the circuit? [16]

7. For the circuit shown in figure 8 , make a plot of V_0 against V_i for the range of V_i from 0 to 50V. Indicate all slopes and voltage levels, and diode conducting region. Assume ideal diodes. [16]

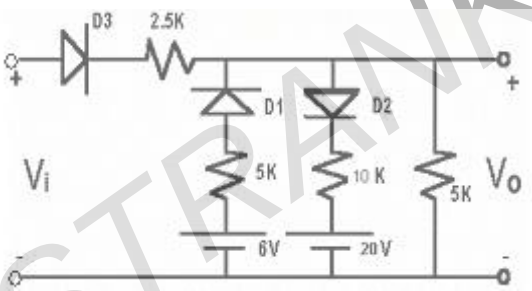

Figure 8

8. (a) Distinguish between logic gate and sampling gate. [4]

   (b) Why is a sampling referred as a linear gate? [4]

   (c) Illustrate the principle of operation of a linear gate using series switch and shunts witch. What are the disadvantages? [8]

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Code No: NR/RR 221003 | **NR/RR** | Set No. 4

II B.Tech II Semester Examinations,December 2010
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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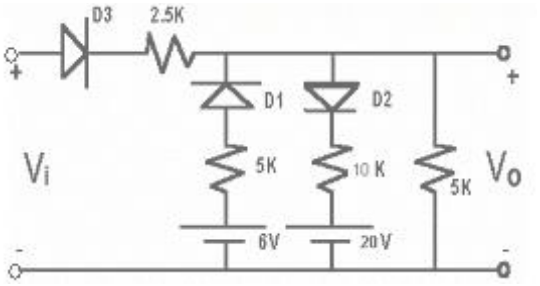

Figure 8

4. (a) Distinguish between logic gate and sampling gate. [4]
   (b) Why is a sampling referred as a linear gate? [4]
   (c) Illustrate the principle of operation of a linear gate using series switch and shunts witch. What are the disadvantages? [8]

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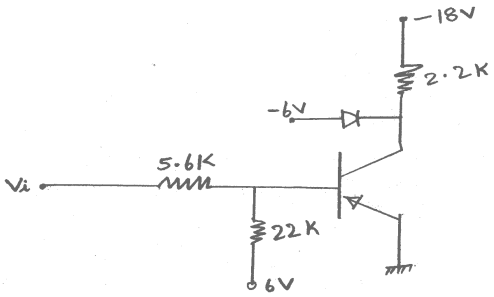
NR/RR

Set No. 4



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8. Explain the operation of an RC controlled free running blocking oscillator with neat sketch of circuit and voltage waveforms. Derive the expression for duty cycle. What are the advantages of the circuit? [16]

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Code No: NR/RR 221003 **NR/RR** Set No. 1

II B.Tech II Semester Examinations,December 2010
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Time: 3 hours **Max Marks: 80**

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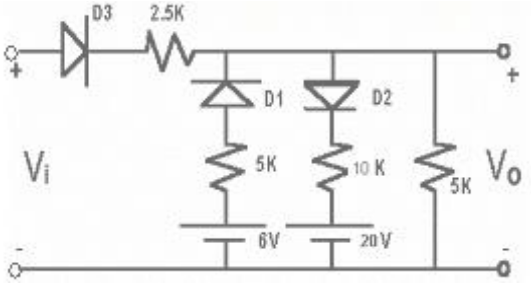

Figure 8

6. (a) Illustrate the terms 'synchronization' and 'frequency division' of a sweep generator. [8]

   (b) A free-running relaxation oscillator has sweep amplitude of 100 V and a period of 1 msec synchronizing pulses are applied to the device such that breakdown voltage is lowered by 50 V at each pulse. The synchronizing pulse frequency is 4 kHz. What is the amplitude and frequency of synchronized oscillator waveform? [8]

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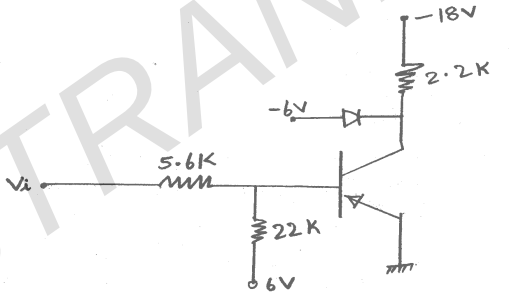

Figure 2a

   (b) Write about diode switching times. [8]

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Code No: NR/RR 221003 | **NR/RR** | Set No. 3

II B.Tech II Semester Examinations,December 2010
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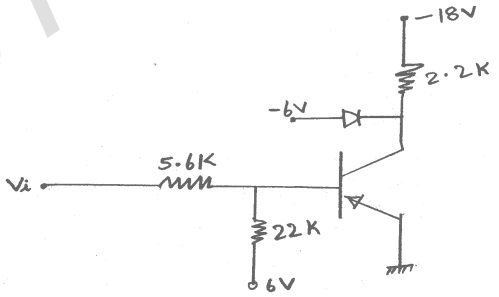

Figure 2a

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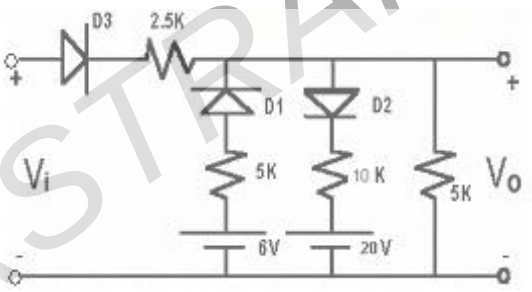

Figure 8

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