Code No: NR/RR210203 | NR/RR | Set No. 2

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to IT, E.COMP.E, ETM, E.CONT.E, EIE, CSE, ECE, CSSE, EEE
Time: 3 hours **Max Marks: 80**
Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Design a BCD adder circuit and given its block schematic and explain its operation with example.
   (b) Realize the following functions using two half adders:
      i. $f_1 = A \oplus B$
      ii. $f_2 = A \oplus B \oplus C$
      iii. $f_3 = (A \oplus B).(AB)$.

      Use additional gates if necessary. [8+8]

2. (a) Explain the limitations of finite-state machines.
   (b) Find the equivalence partition and a corresponding reduced machine in standard form for the machine given below: [6+10]

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

3. Construct an ASM block that has 3 input variables (D,E,F) and 4 output variables (P,Q,R,S) and 2 exit paths. For this block, output P is always 1, and Q is 1 if D=1. If D & F are 1 or if D & E are 0, R=1 and exit path 2 is taken. If (D=0 & E=1) or (D=1 & F=0), S=1 and exit path 1 is taken.
   Realize it with One flip flop per state. [16]

4. (a) With the help of block-diagrams, explain the difference between synchronous sequential circuit and Asynchronous sequential circuit and compare them.
   (b) For the block diagram(figure6b) shown below, draw the schematic circuit using NAND gates and explain its working with the help of Truth-Table. [6+10]

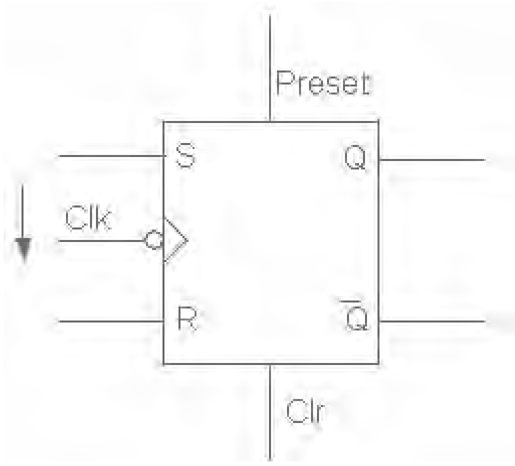

Figure 6b

5. (a) Simplify the function using Karnaugh map method
F (A,B,C,D) = $\sum$(4,5,7,12,14,15)+ $\sum$d(3,8,10).

(b) Give three possible ways to express the function
F = $\overline{A}\ \overline{B}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}BD + AB\overline{C}D$ with eight or less literals. [8+8]

6. (a) Derive Boolean expression for a 2input Ex-OR gate to realize with 2 input NAND gates without using complemented variables and draw the circuit.

(b) Redraw the given circuit in (figure4b)after simplification. [8+8]

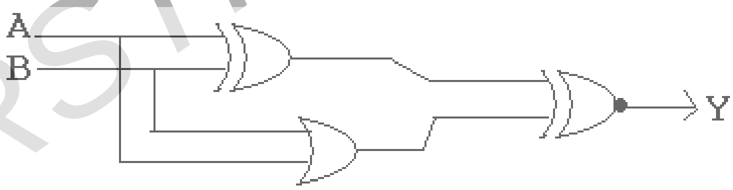

Figure 4b

7. Derive the state diagram and state table for two input(x_1, x_2) and single output z asynchronous circuit. The output of the circuit $z = x_1$ if $x_2 = 1$, but if $x_2 = 0$, the output is to remain fixed at its last value before x_2 becomes zero and design the circuit using D-flip flops. [16]

8. (a) Consider the following four codes.

Code A		Code B		Code C		Code D	
0001		000		01011		000000	
0010		001		01100		001111	
0100	2	011	1	10010	3	110011	4
1000		010		10101			
		110					
		111					
		101					
		100					

Which of the following properties is satisfied by each of the above codes?

i. Detects single errors
ii. Detects double errors
iii. Detects triple errors
iv. Corrects single errors
v. Corrects double errors
Corrects singe and detects double errors.

(b) Add the following decimal number 109 and 876 in BCD and Excess-3 forms. [8+8]

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Code No: NR/RR210203 **NR/RR** **Set No. 4**

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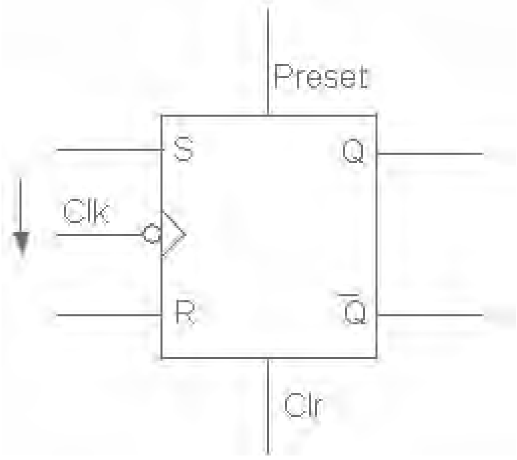

Figure 6b

4. Construct an ASM block that has 3 input variables (D,E,F) and 4 output variables (P,Q,R,S) and 2 exit paths. For this block, output P is always 1, and Q is 1 if D=1. If D & F are 1 or if D & E are 0, R=1 and exit path 2 is taken. If (D=0 & E=1) or (D=1 & F=0), S=1 and exit path 1 is taken.
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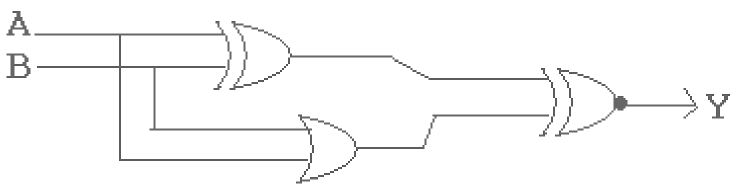

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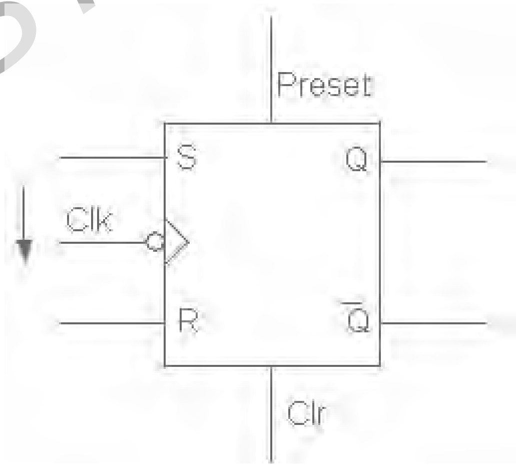

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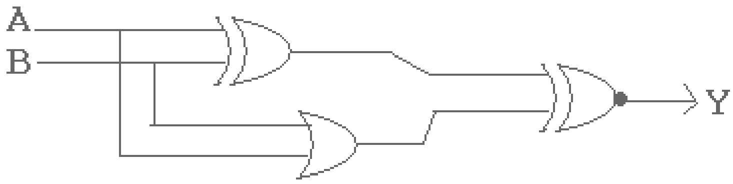

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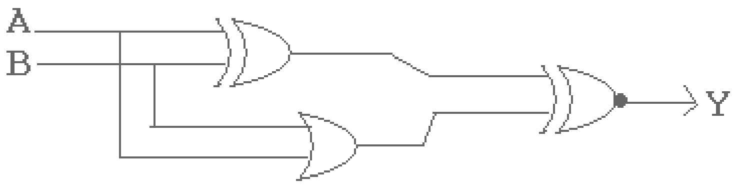

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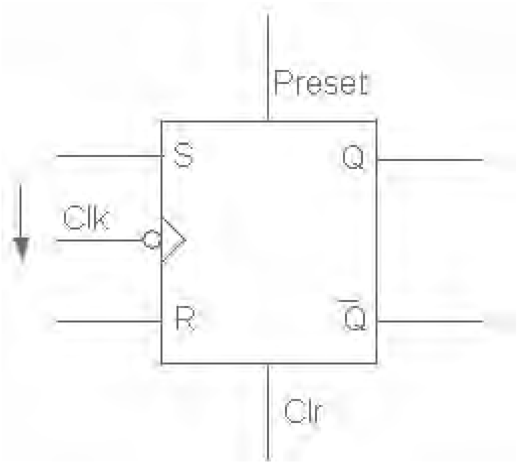

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