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Code No: NR220203 **NR** **Set No. 2**

II B.Tech II Semester Examinations,December 2010
LINEAR DIGITAL I.C. APPLICATIONS
Common to Electronics And Computer Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give the block diagram of 565 PLL (DIP) and explain about each block and for the given component values find the free running frequency f_o, lock-range and capture range C_1=470PF; C_2=1000PF, R_1=10k and V_{CC}= $\pm$ 6V
   C_1 connected between pin 9 and $-V_{CC}$
   C_2 connected between pin 7 and $+V_{CC}$. [8]
   (b) Give any two applications of PLL and explain about each one in detail. [8]

2. (a) What is a sample-and-hold circuit? Draw the circuit diagram and explain its action? [6]
   (b) With reference to sample and hold circuit define the following terms: [4]
      i. Aperture time
      ii. Hold mode.
   (c) Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage V_o. [6]

3. Write short notes on the following gates :
   (a) TTL [6]
   (b) I^2 L [4]
   (c) ECL [6]

4. (a) Discuss the applications of Op-Amp combines with a PN junction diode. [8]
   (b) Explain the operation of a scale changer with circuit diagram. [8]

5. Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer. [16]

6. (a) Define the terms : SVRR,CMRR, input bias current, input offset voltage, Gain Bandwidth product [10]
   (b) What are the differences between the inverting and non inverting terminals? What do you mean by the term ''virtual ground''? [6]

7. (a) Derive an expression for the quality factor 'Q' of a twin-T notch filter. Give the suitable circuit diagram. [8]

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(b) Identify the given circuit(figure7b) and derive an expression for Bandwidth of the same circuit. [8]

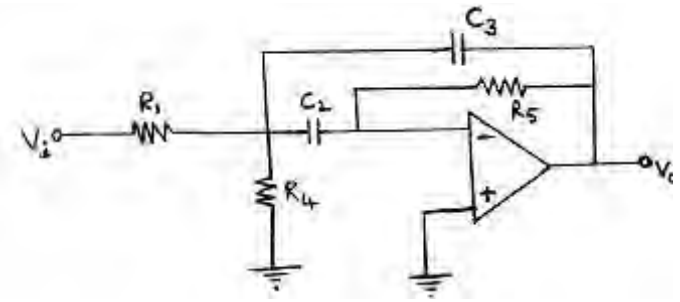

Figure 7b

8. (a) What feedback is preferred for oscillators and why? What is the effect of negative feedback? [8]

(b) Design an OP-AMP based relaxation oscillator and derive the frequency of oscillation. [8]

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Code No: NR220203 **NR** **Set No. 4**

II B.Tech II Semester Examinations,December 2010
LINEAR DIGITAL I.C. APPLICATIONS
Common to Electronics And Computer Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive an expression for the quality factor 'Q' of a twin-T notch filter. Give the suitable circuit diagram. [8]
   (b) Identify the given circuit(figure 1b) and derive an expression for Bandwidth of the same circuit. [8]

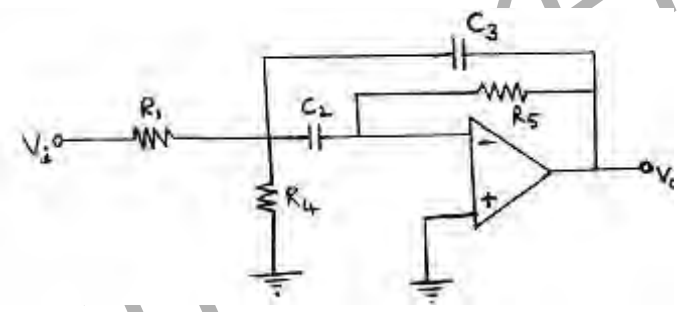

Figure 1b

2. Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer. [16]

3. (a) Give the block diagram of 565 PLL (DIP) and explain about each block and for the given component values find the free running frequency f_o, lock-range and capture range C_1=470PF; C_2=1000PF, R_1=10k and V_{CC}= ± 6V
   C_1 connected between pin 9 and $-V_{CC}$
   C_2 connected between pin 7 and $+V_{CC}$. [8]
   (b) Give any two applications of PLL and explain about each one in detail. [8]

4. (a) What is a sample-and-hold circuit? Draw the circuit diagram and explain its action? [6]
   (b) With reference to sample and hold circuit define the following terms: [4]
      i. Aperture time
      ii. Hold mode.
   (c) Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage V_o. [6]

5. (a) What feedback is preferred for oscillators and why? What is the effect of negative feedback? [8]
   (b) Design an OP-AMP based relaxation oscillator and derive the frequency of oscillation. [8]

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6. (a) Discuss the applications of Op-Amp combines with a PN junction diode. [8]
   (b) Explain the operation of a scale changer with circuit diagram. [8]

7. Write short notes on the following gates :
   (a) TTL [6]
   (b) I^2 L [4]
   (c) ECL [6]

8. (a) Define the terms : SVRR,CMRR, input bias current, input offset voltage, Gain Bandwidth product [10]
   (b) What are the differences between the inverting and non inverting terminals? What do you mean by the term ''virtual ground''? [6]

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Code No: NR220203 **NR** **Set No. 1**

II B.Tech II Semester Examinations,December 2010
LINEAR DIGITAL I.C. APPLICATIONS
Common to Electronics And Computer Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer. [16]
2. Write short notes on the following gates :
   (a) TTL [6]
   (b) I^2 L [4]
   (c) ECL [6]
3. (a) What is a sample-and-hold circuit? Draw the circuit diagram and explain its action? [6]
   (b) With reference to sample and hold circuit define the following terms: [4]
      i. Aperture time
      ii. Hold mode.
   (c) Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage V_o. [6]
4. (a) Give the block diagram of 565 PLL (DIP) and explain about each block and for the given component values find the free running frequency f_o, lock-range and capture range C_1=470PF; C_2=1000PF, R_1=10k and V_{CC}= ± 6V
   C_1 connected between pin 9 and $-V_{CC}$
   C_2 connected between pin 7 and $+V_{CC}$. [8]
   (b) Give any two applications of PLL and explain about each one in detail. [8]
5. (a) Derive an expression for the quality factor 'Q' of a twin-T notch filter. Give the suitable circuit diagram. [8]
   (b) Identify the given circuit(figure 5b) and derive an expression for Bandwidth of the same circuit. [8]

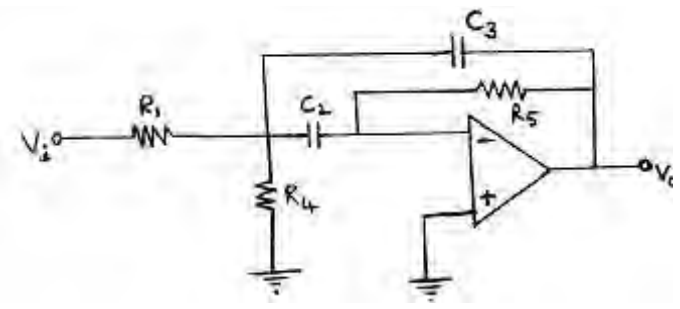

Figure 5b

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6. (a) Discuss the applications of Op-Amp combines with a PN junction diode. [8]
   (b) Explain the operation of a scale changer with circuit diagram. [8]

7. (a) Define the terms : SVRR,CMRR, input bias current, input offset voltage, Gain Bandwidth product [10]
   (b) What are the differences between the inverting and non inverting terminals? What do you mean by the term ''virtual ground''? [6]

8. (a) What feedback is preferred for oscillators and why? What is the effect of negative feedback? [8]
   (b) Design an OP-AMP based relaxation oscillator and derive the frequency of oscillation. [8]

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Code No: NR220203 **NR** **Set No. 3**

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Common to Electronics And Computer Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define the terms : SVRR,CMRR, input bias current, input offset voltage, Gain Bandwidth product [10]
   (b) What are the differences between the inverting and non inverting terminals? What do you mean by the term ''virtual ground''? [6]
2. (a) What feedback is preferred for oscillators and why? What is the effect of negative feedback? [8]
   (b) Design an OP-AMP based relaxation oscillator and derive the frequency of oscillation. [8]
3. Write short notes on the following gates :
   (a) TTL [6]
   (b) I^2 L [4]
   (c) ECL [6]
4. (a) Discuss the applications of Op-Amp combines with a PN junction diode. [8]
   (b) Explain the operation of a scale changer with circuit diagram. [8]
5. (a) What is a sample-and-hold circuit? Draw the circuit diagram and explain its action? [6]
   (b) With reference to sample and hold circuit define the following terms: [4]
      i. Aperture time
      ii. Hold mode.
   (c) Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage V_o. [6]
6. Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer. [16]
7. (a) Derive an expression for the quality factor 'Q' of a twin-T notch filter. Give the suitable circuit diagram. [8]
   (b) Identify the given circuit(figure7b) and derive an expression for Bandwidth of the same circuit. [8]

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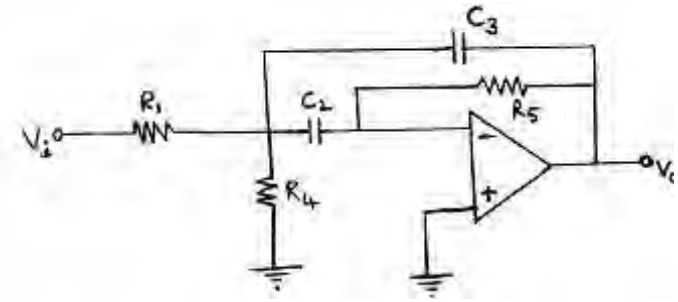

Figure 7b

8. (a) Give the block diagram of 565 PLL (DIP) and explain about each block and for the given component values find the free running frequency f_o, lock-range and capture range C_1=470PF; C_2=1000PF, R_1=10k and V_{CC}= $\pm$ 6V
   C_1 connected between pin 9 and $-V_{CC}$
   C_2 connected between pin 7 and $+V_{CC}$. [8]
   (b) Give any two applications of PLL and explain about each one in detail. [8]

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