Code No: NR320202 **NR** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO-CONTROLLERS
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are Register windows and how are they implemented in RISC machines? [8]
   (b) Distinguish between pipelining and super-pipelining? [8]
2. (a) Explain the terms: [3+4]
      i. Baud rate in the 8051
      ii. SCON register
   (b) List out the steps involved in programming the 8051 to transfer data serially. [9]
3. (a) Write an 8085 assembly language program to add two 24 bit numbers. [6]
   (b) Write an 8086 assembly program to add N number of 16-bit numbers stored in consecutive memory locations starting at 0500H in the data segment 0200H. Store the result onto the stack. [10]
4. Explain in detail about the 80486 memory management unit. [16]
5. (a) Explain the following instructions of MC 68000
      i. BFCHG
      ii. BSR
      iii. CAS2
      iv. FBCC
      v. SUBA
   (b) Explain how different data sizes are handled in MC 68000? Explain.
   (c) How many address spaces does 68000 provide and how I/O devices are addressed? [5+6+5]
6. (a) Explain the stack operation in 8051 microcontroller? [8]
   (b) Discuss how the CPU uses the stack to store CALL and RET addresses? [8]
7. (a) Explain the various stages involved in the development of Pentium based systems? [8]
   (b) Explain the use of in circuit emulator in a development system? Discuss ICE for Pentium based system development? [8]
8. (a) Explain the features of Level 1 instruction and data caches of Pentium microprocessor. [7]

(b) Discuss the functions of branch prediction and Branch Target Buffer of Pentium microprocessor. [9]

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Code No: NR320202 **NR** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO-CONTROLLERS
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the stack operation in 8051 microcontroller? [8]
   (b) Discuss how the CPU uses the stack to store CALL and RET addresses? [8]
2. (a) Explain the features of Level 1 instruction and data caches of Pentium microprocessor. [7]
   (b) Discuss the functions of branch prediction and Branch Target Buffer of Pentium microprocessor. [9]
3. (a) Write an 8085 assembly language program to add two 24 bit numbers. [6]
   (b) Write an 8086 assembly program to add N number of 16-bit numbers stored in consecutive memory locations starting at 0500H in the data segment 0200H. Store the result onto the stack. [10]
4. (a) Explain the various stages involved in the development of Pentium based systems? [8]
   (b) Explain the use of in circuit emulator in a development system? Discuss ICE for Pentium based system development? [8]
5. (a) Explain the following instructions of MC 68000
      i. BFCHG
      ii. BSR
      iii. CAS2
      iv. FBCC
      v. SUBA
   (b) Explain how different data sizes are handled in MC 68000? Explain.
   (c) How many address spaces does 68000 provide and how I/O devices are addressed? [5+6+5]
6. (a) What are Register windows and how are they implemented in RISC machines? [8]
   (b) Distinguish between pipelining and super-pipelining? [8]
7. (a) Explain the terms: [3+4]
      i. Baud rate in the 8051
      ii. SCON register

(b) List out the steps involved in programming the 8051 to transfer data serially. [9]

8. Explain in detail about the 80486 memory management unit. [16]

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Code No: NR320202 **NR** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO-CONTROLLERS
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the following instructions of MC 68000
   i. BFCHG
   ii. BSR
   iii. CAS2
   iv. FBCC
   v. SUBA
   (b) Explain how different data sizes are handled in MC 68000? Explain.
   (c) How many address spaces does 68000 provide and how I/O devices are addressed? [5+6+5]
2. (a) What are Register windows and how are they implemented in RISC machines? [8]
   (b) Distinguish between pipelining and super-pipelining? [8]
3. (a) Write an 8085 assembly language program to add two 24 bit numbers. [6]
   (b) Write an 8086 assembly program to add N number of 16-bit numbers stored in consecutive memory locations starting at 0500H in the data segment 0200H. Store the result onto the stack. [10]
4. (a) Explain the stack operation in 8051 microcontroller? [8]
   (b) Discuss how the CPU uses the stack to store CALL and RET addresses? [8]
5. Explain in detail about the 80486 memory management unit. [16]
6. (a) Explain the various stages involved in the development of Pentium based systems? [8]
   (b) Explain the use of in circuit emulator in a development system? Discuss ICE for Pentium based system development? [8]
7. (a) Explain the features of Level 1 instruction and data caches of Pentium microprocessor. [7]
   (b) Discuss the functions of branch prediction and Branch Target Buffer of Pentium microprocessor. [9]
8. (a) Explain the terms: [3+4]
   i. Baud rate in the 8051

ii. SCON register

(b) List out the steps involved in programming the 8051 to transfer data serially. [9]

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Code No: NR320202 **NR** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO-CONTROLLERS
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Write an 8085 assembly language program to add two 24 bit numbers. [6]
   (b) Write an 8086 assembly program to add N number of 16-bit numbers stored in consecutive memory locations starting at 0500H in the data segment 0200H. Store the result onto the stack. [10]
2. (a) What are Register windows and how are they implemented in RISC machines? [8]
   (b) Distinguish between pipelining and super-pipelining? [8]
3. (a) Explain the various stages involved in the development of Pentium based systems? [8]
   (b) Explain the use of in circuit emulator in a development system? Discuss ICE for Pentium based system development? [8]
4. (a) Explain the features of Level 1 instruction and data caches of Pentium microprocessor. [7]
   (b) Discuss the functions of branch prediction and Branch Target Buffer of Pentium microprocessor. [9]
5. (a) Explain the terms: [3+4]
      i. Baud rate in the 8051
      ii. SCON register
   (b) List out the steps involved in programming the 8051 to transfer data serially. [9]
6. (a) Explain the stack operation in 8051 microcontroller? [8]
   (b) Discuss how the CPU uses the stack to store CALL and RET addresses? [8]
7. (a) Explain the following instructions of MC 68000
      i. BFCHG
      ii. BSR
      iii. CAS2
      iv. FBCC
      v. SUBA
   (b) Explain how different data sizes are handled in MC 68000? Explain.

(c) How many address spaces does 68000 provide and how I/O devices are addressed? [5+6+5]

8. Explain in detail about the 80486 memory management unit. [16]

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