Code No: NR320404 **NR** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
VLSI TECHNOLOGY
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain channel formation in case of depletion mode MOS transistors and how the transistor action differs from enhancement mode transistor.
   (b) Explain how a bi polar npn transistor is included in n well CMOS processing. Draw the cross section of Bi CMOS transistor. [6+10]
2. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.
   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain. [8+8]
3. Explain about the design approaches for full custom and semi custom Devices. [16]
4. (a) Explain the various methods used to test sequential Logic.
   (b) Distinguish between simulator and circuit extractor. [8+8]
5. (a) Write a note on the general observation about design rules.
   (b) What are contact cuts? Explain buried and but contacts with cross sectional and top view diagrams. [8+8]
6. (a) Explain ceramic package types with their cross sectional sketches.
   (b) Why package sealing is required in packing and how it is done? [8+8]
7. (a) What are the different types of programmable inter connection channels used for routing parts in FPGAs? Explain.
   (b) Explain about anti fuses used in FPGAs. [8+8]
8. Briefly explain the following verification tools:
   (a) timing verifiers
   (b) design rule checkers
   (c) layout extractions and
   (d) test vectors. [4+4+4+4]

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Code No: NR320404 **NR** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
VLSI TECHNOLOGY
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Write a note on the general observation about design rules.
   (b) What are contact cuts? Explain buried and but contacts with cross sectional and top view diagrams. [8+8]
2. Briefly explain the following verification tools:
   (a) timing verifiers
   (b) design rule checkers
   (c) layout extractions and
   (d) test vectors. [4+4+4+4]
3. (a) What are the different types of programmable inter connection channels used for routing parts in FPGAs? Explain.
   (b) Explain about anti fuses used in FPGAs. [8+8]
4. (a) Explain ceramic package types with their cross sectional sketches.
   (b) Why package sealing is required in packing and how it is done? [8+8]
5. (a) Explain the various methods used to test sequential Logic.
   (b) Distinguish between simulator and circuit extractor. [8+8]
6. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.
   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain. [8+8]
7. (a) Explain channel formation in case of depletion mode MOS transistors and how the transistor action differs from enhancement mode transistor.
   (b) Explain how a bi polar npn transistor is included in n well CMOS processing. Draw the cross section of Bi CMOS transistor. [6+10]
8. Explain about the design approaches for full custom and semi custom Devices. [16]

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Code No: NR320404 **NR** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
VLSI TECHNOLOGY
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Briefly explain the following verification tools:
   (a) timing verifiers
   (b) design rule checkers
   (c) layout extractions and
   (d) test vectors. [4+4+4+4]
2. (a) What are the different types of programmable inter connection channels used for routing parts in FPGAs? Explain.
   (b) Explain about anti fuses used in FPGAs. [8+8]
3. (a) Explain ceramic package types with their cross sectional sketches.
   (b) Why package sealing is required in packing and how it is done? [8+8]
4. (a) Explain channel formation in case of depletion mode MOS transistors and how the transistor action differs from enhancement mode transistor.
   (b) Explain how a bi polar npn transistor is included in n well CMOS processing. Draw the cross section of Bi CMOS transistor. [6+10]
5. Explain about the design approaches for full custom and semi custom Devices. [16]
6. (a) Write a note on the general observation about design rules.
   (b) What are contact cuts? Explain buried and but contacts with cross sectional and top view diagrams. [8+8]
7. (a) Explain the various methods used to test sequential Logic.
   (b) Distinguish between simulator and circuit extractor. [8+8]
8. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.
   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain. [8+8]

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Code No: NR320404 **NR** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
VLSI TECHNOLOGY
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.
   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain. [8+8]
2. (a) Write a note on the general observation about design rules.
   (b) What are contact cuts? Explain buried and but contacts with cross sectional and top view diagrams. [8+8]
3. (a) What are the different types of programmable inter connection channels used for routing parts in FPGAs? Explain.
   (b) Explain about anti fuses used in FPGAs. [8+8]
4. (a) Explain ceramic package types with their cross sectional sketches.
   (b) Why package sealing is required in packing and how it is done? [8+8]
5. Briefly explain the following verification tools:
   (a) timing verifiers
   (b) design rule checkers
   (c) layout extractions and
   (d) test vectors. [4+4+4+4]
6. Explain about the design approaches for full custom and semi custom Devices. [16]
7. (a) Explain the various methods used to test sequential Logic.
   (b) Distinguish between simulator and circuit extractor. [8+8]
8. (a) Explain channel formation in case of depletion mode MOS transistors and how the transistor action differs from enhancement mode transistor.
   (b) Explain how a bi polar npn transistor is included in n well CMOS processing. Draw the cross section of Bi CMOS transistor. [6+10]

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