Code No: R05210204 **R05** **Set No. 2**

II B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain, How error occurred in a data transmission can be detected using parity bit. [6]
   (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. [5 × 2 = 10]
      i. 101011 - 111000
      ii. 1110 - 110010
      iii. 11010 - 1101
      iv. 110 - 101000
      v. 11010 - 10000

2. Minimise on the map the five variable function.
   F= $\sum m(0, 1, 4, 5, 6, 13, 14, 15, 22, 24, 25, 28, 29, 30, 31)$. [16]

3. A Clocked sequential circuit with two inputs x and y and a single output Z using J - K flip flops is as shown in figure 7:

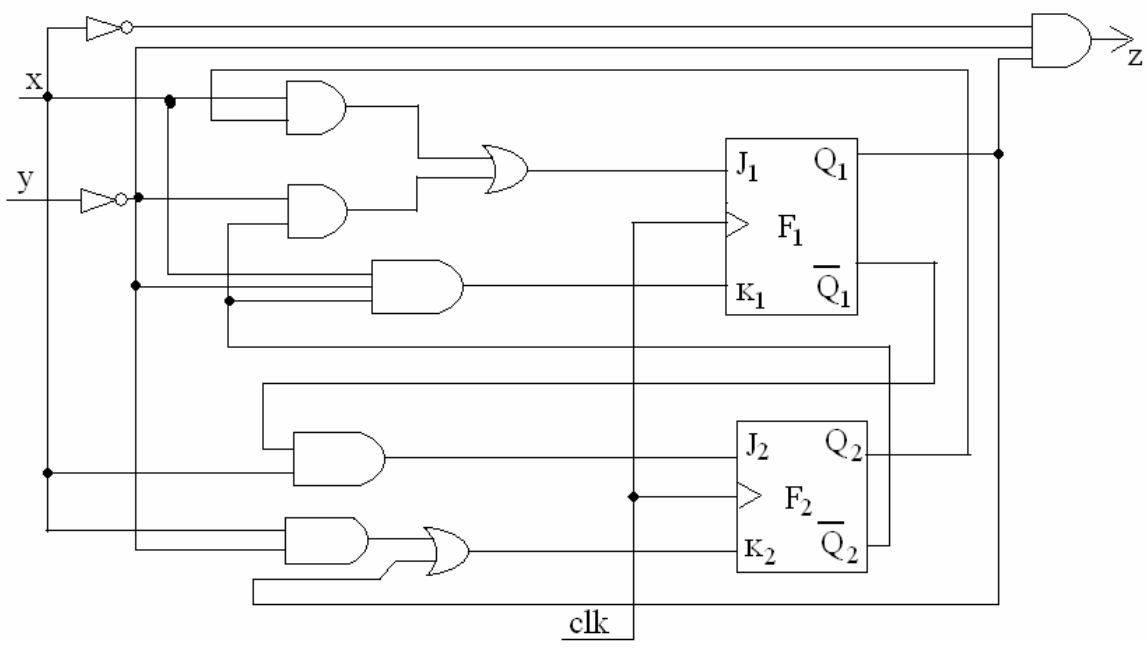

Figure 7

(a) Obtain input equations.

(b) List the state table

(c) Draw the corresponding state diagram.

(d) Derive state - equations. [4+4+4+4]

4. (a) List the PLA programming table for the BCD to excess-3 code converter.

(b) A ROM chip of 4,096 × 8 bits has two clip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit package? Draw the block diagram of this ROM. [8+8]

5. For the ASM chart given below figure 8:

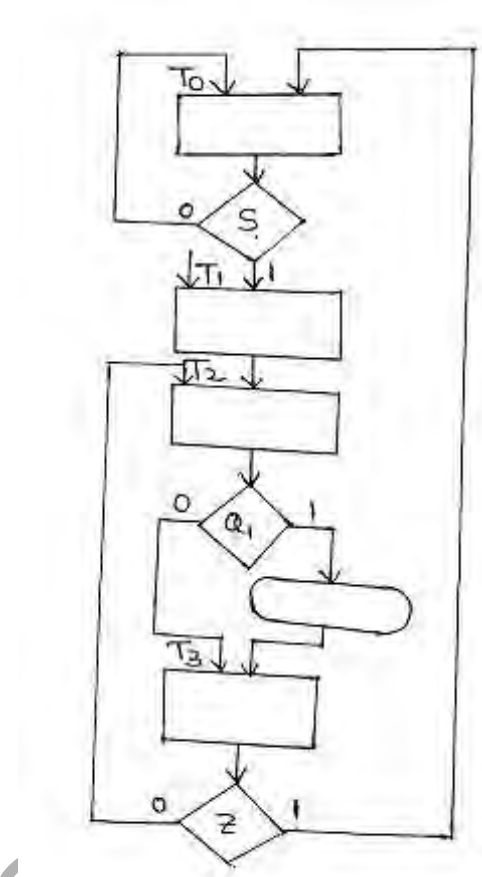

Figure 8

(a) Draw the state diagram.

(b) Design the control unit using D flip-flops and a decoder. [8+8]

6. (a) Using the method of flip flop conversion carry out the following conversions.
   i. S-R to T
   ii. J-K to D [4x2=8]

   (b) Verify the circuit and explain its function. With the timing waveforms. Shown in figure 1 [8]

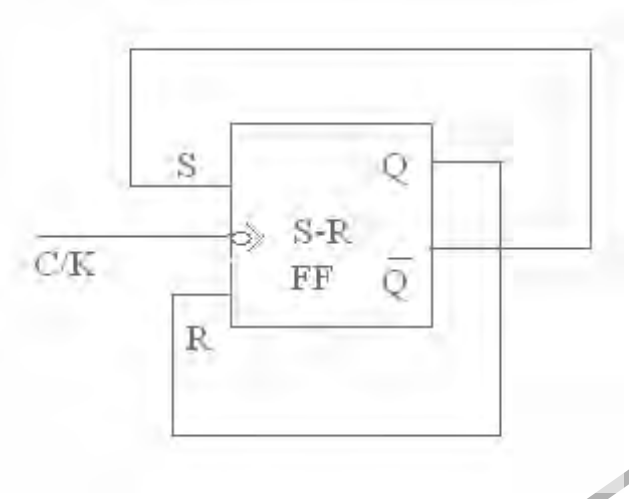

Figure 1

7. (a) Simplify the following expressions and implement them with NAND gate circuits. [8]
   i. AB'+ABD+ABD'+A'C'D'+A'BC'
   ii. BD+BCD'+AB'C'D'
   (b) Obtain the Dual of the following Boolean expressions.
   i. AB+A(B+C)+B'(B+D)
   ii. A+B+A'B'C [4]
   (c) Obtain the complement of the following Boolean expressions.
   i. A'B+A'BC'+A'BCD+A'BC'D'E
   ii. ABEF+ABE'F'+A'B'EF [4]
8. Design and implement a Binary to Gray converter. [16]

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Code No: R05210204 **R05** **Set No. 4**

II B.Tech I Semester Examinations,November 2010
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Time: 3 hours **Max Marks: 80**

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⋆ ⋆ ⋆ ⋆ ⋆

1. A Clocked sequential circuit with two inputs x and y and a single output Z using J - K flip flops is as shown in figure 7:

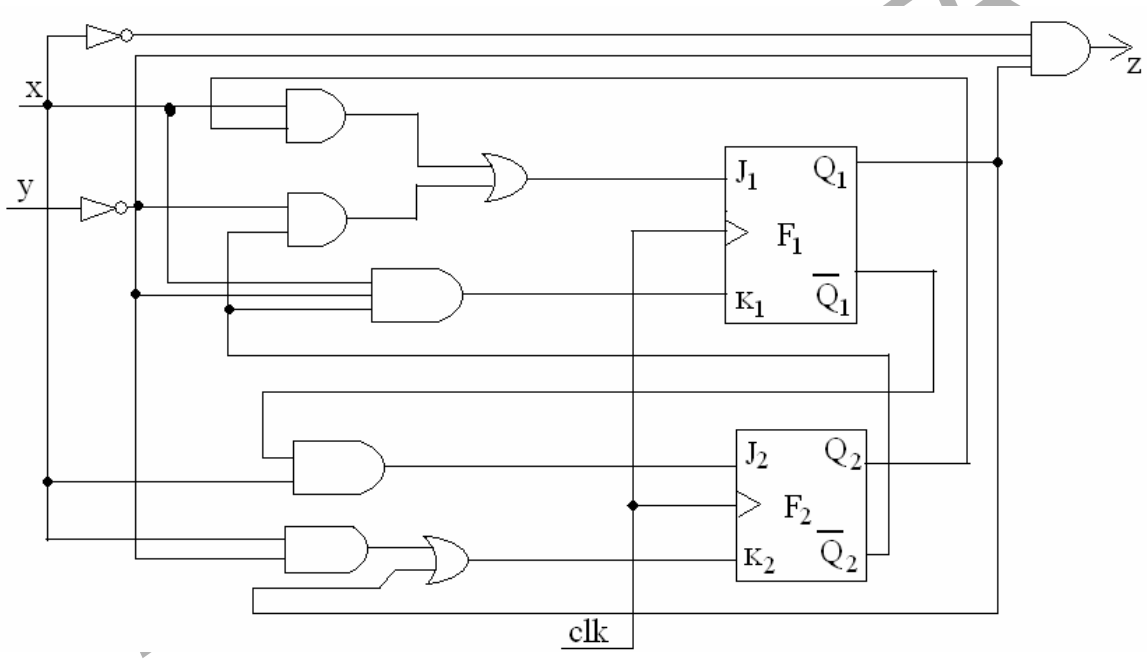

Figure 7

   (a) Obtain input equations.
   (b) List the state table
   (c) Draw the corresponding state diagram.
   (d) Derive state - equations. [4+4+4+4]

2. Minimise on the map the five variable function.
   F= $\sum m(0, 1, 4, 5, 6, 13, 14, 15, 22, 24, 25, 28, 29, 30, 31)$. [16]

3. (a) Using the method of flip flop conversion carry out the following conversions.
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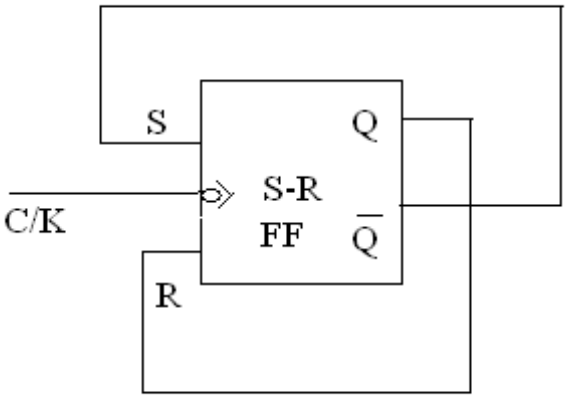

Figure 1

4. Design and implement a Binary to Gray converter. [16]

5. (a) List the PLA programming table for the BCD to excess-3 code converter.

(b) A ROM chip of 4,096 × 8 bits has two clip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit package? Draw the block diagram of this ROM. [8+8]

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(b) Obtain the Dual of the following Boolean expressions.

i. AB+A(B+C)+B'(B+D)

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(b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. [5 × 2 = 10]

i. 101011 - 111000

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8. For the ASM chart given below figure 8:

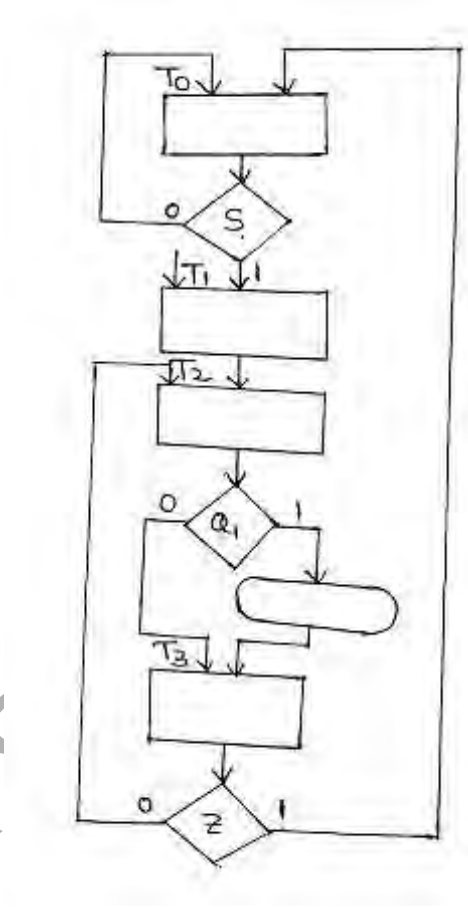

Figure 8

(a) Draw the state diagram.
(b) Design the control unit using D flip-flops and a decoder. [8+8]

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Code No: R05210204 **R05** **Set No. 1**

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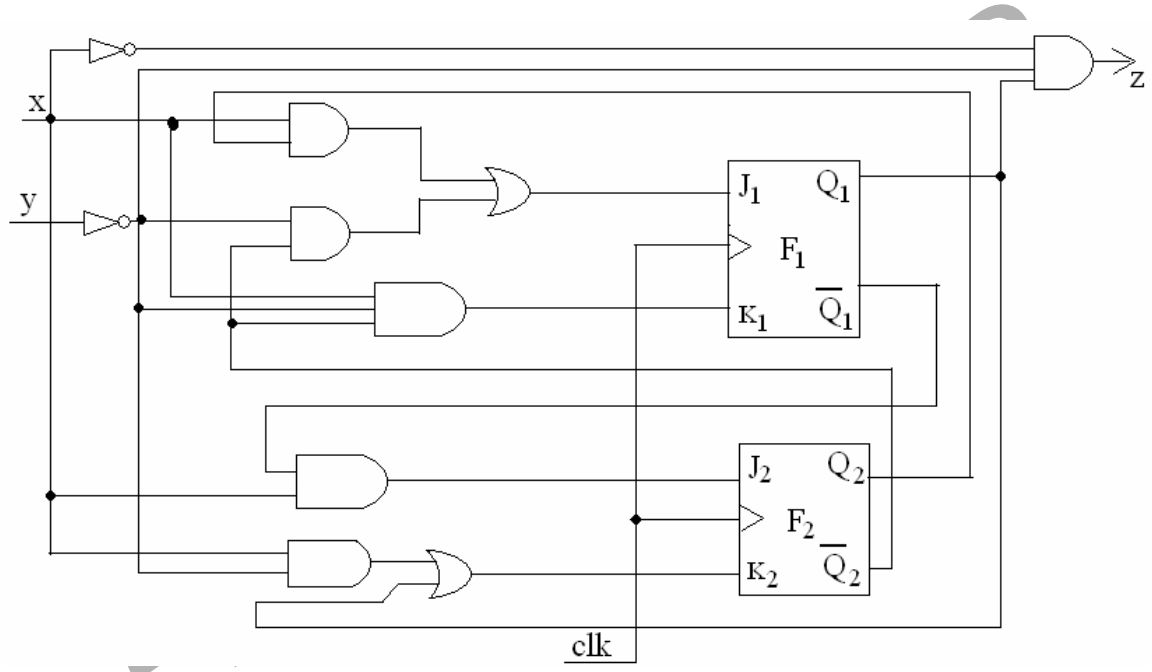

Figure 7

   (a) Obtain input equations.
   (b) List the state table
   (c) Draw the corresponding state diagram.
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2. (a) Simplify the following expressions and implement them with NAND gate circuits. [8]
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4. Design and implement a Binary to Gray converter. [16]

5. (a) Using the method of flip flop conversion carry out the following conversions.
i. S-R to T
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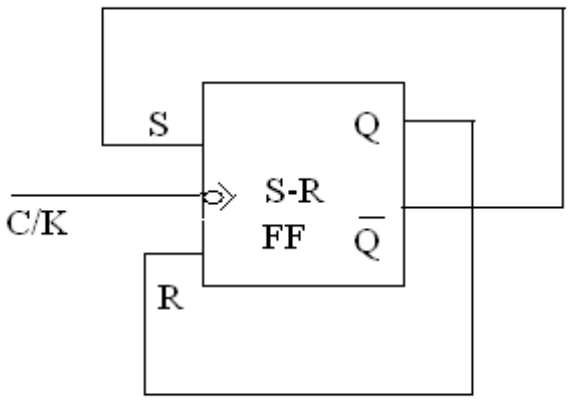

Figure 1

6. For the ASM chart given below figure 8:

Code No: R05210204 **R05** **Set No. 1**

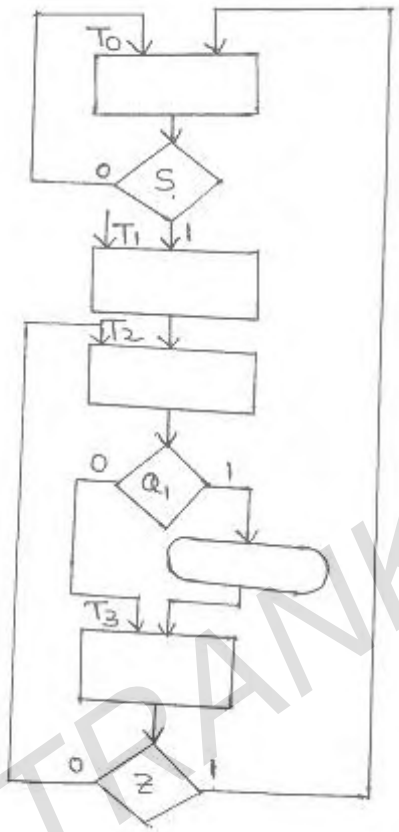

Figure 8

(a) Draw the state diagram.

(b) Design the control unit using D flip-flops and a decoder. [8+8]

7. (a) List the PLA programming table for the BCD to excess-3 code converter.

(b) A ROM chip of 4,096 × 8 bits has two clip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit package? Draw the block diagram of this ROM. [8+8]

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Code No: R05210204 **R05** **Set No. 3**

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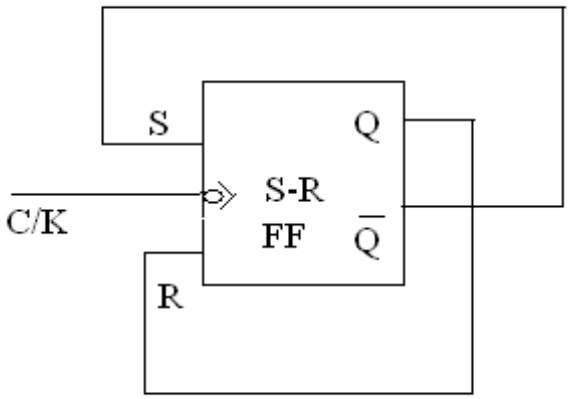

Figure 1

2. (a) List the PLA programming table for the BCD to excess-3 code converter.
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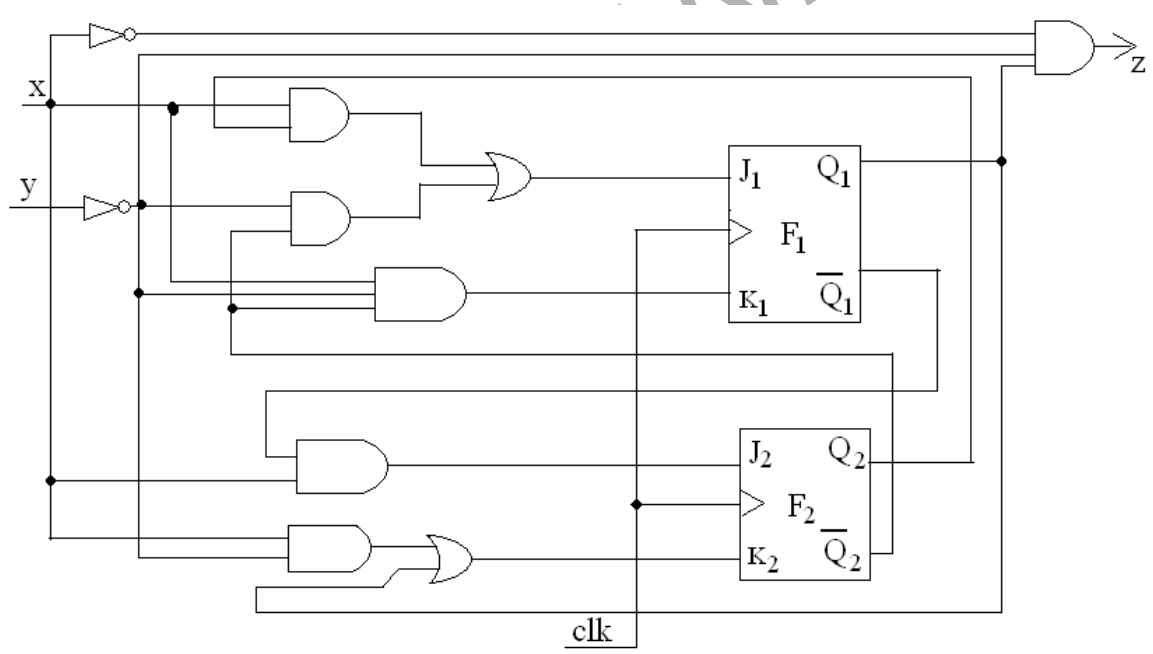

Figure 7

   (a) Obtain input equations.
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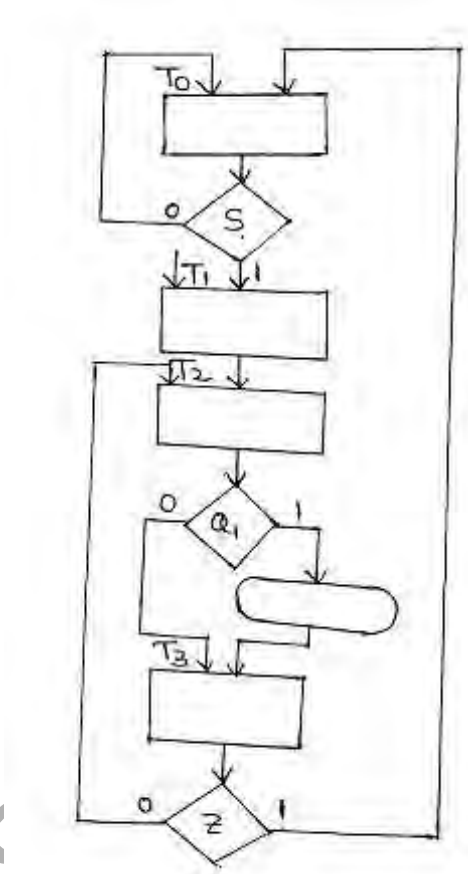

Figure 8

(a) Draw the state diagram.

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