Code No: R05210504 **R05** **Set No. 2**

II B.Tech I Semester Examinations,November 2010
DIGITAL LOGIC DESIGN
Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define the following terms related to filp-flops.
   i. set-up time
   ii. hold time
   iii. propagation delay
   iv. preset and
   v. clear.
   (b) Distinguish between combinational logic and sequential logic. [10+6]
2. (a) Draw and explain 4-bit universal shift register.
   (b) Explain different types of shift registers. [8+8]
3. (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.
   (b) i. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes.
   ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
   iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder. [8+8]
4. (a) List the first 20 numbers in base17. Use the letters A, B, C, D, E, F and G to represent the last seven digits. [4]
   (b) Convert the following numbers with the given radix to decimal.
   i. 1234_5
   ii. 1234_7
   iii. 1234_{11}
   iv. 333_4 [3+3+3+3]
5. (a) Describe the analysis procedure of asynchronous sequential logic using flow table
   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are: [6+10]

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$z = x_2 + y_1$$

i. Draw the logic diagram of the circuit.
ii. Derive the transition table and output map.
iii. Obtain a flow table for the circuit.

6. (a) Explain the concept of positive logic and negative logic. Also draw the truth tables for positive logic AND gate and negative logic OR gate.

(b) Obtain the complement of the following Boolean expressions.
i. B'C'D + (B + C + D)' + B'C'D'E
ii. AB + (AC)' + (AB + C).

(c) Obtain the dual of the following Boolean expressions. [8+4+4]
i. A'B'C' + A'BC' + AB'C' + ABC'
ii. AB + (AC)' + AB'C.

7. (a) Show that wired circuit (Figure 2a) perform the following function:
$Y = (A \oplus B) \bullet (C \oplus D)$

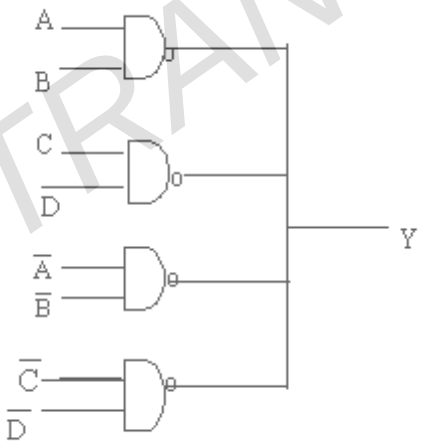

Figure 2a

(b) A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are 1. The function is 0 otherwise. Write the HDL user - defined primitive for 3 bit majority functions. Assume A, B, C are the input variable and Y is the output variable. [8+8]

8. (a) Using five lower - order demultiplexer, construct 6 to 64 line demultiplexer circuit. Use only block diagrams.

(b) Design a Combinational logic circuit with three inputs A, B, C and three outputs x, y, z. If the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Draw the circuit using three-2 input AND gates, one 3 input OR gate, one 3 input X - OR gate and one inverter. [4+12]

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Code No: R05210504 **R05** **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Show that wired circuit (Figure 2a) perform the following function: $Y = (A \oplus B) \bullet (C \oplus D)$

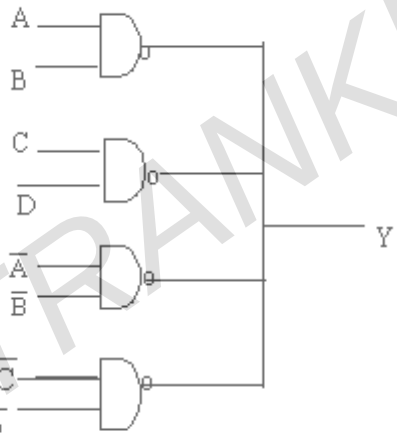

Figure 2a

(b) A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are 1. The function is 0 otherwise. Write the HDL user - defined primitive for 3 bit majority functions. Assume A, B, C are the input variable and Y is the output variable. [8+8]

2. (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.

(b) i. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes.

ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?

iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder. [8+8]

3. (a) Explain the concept of positive logic and negative logic. Also draw the truth tables for positive logic AND gate and negative logic OR gate.

(b) Obtain the complement of the following Boolean expressions.

i. B'C'D + (B + C + D)' + B'C'D'E

ii. AB + (AC)' + (AB + C).

(c) Obtain the dual of the following Boolean expressions. [8+4+4]

i. A'B'C' + A'BC' + AB'C' + ABC'

ii. AB + (AC)' + AB'C.

4. (a) Describe the analysis procedure of asynchronous sequential logic using flow table

(b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are: [6+10]

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$z = x_2 + y_1$$

i. Draw the logic diagram of the circuit.

ii. Derive the transition table and output map.

iii. Obtain a flow table for the circuit.

5. (a) Using five lower - order demultiplexer, construct 6 to 64 line demultiplexer circuit. Use only block diagrams.

(b) Design a Combinational logic circuit with three inputs A, B, C and three outputs x, y, z. If the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Draw the circuit using three-2 input AND gates, one 3 input OR gate, one 3 input X - OR gate and one inverter. [4+12]

6. (a) Draw and explain 4-bit universal shift register.

(b) Explain different types of shift registers. [8+8]

7. (a) Define the following terms related to filp-flops.

i. set-up time

ii. hold time

iii. propagation delay

iv. preset and

v. clear.

(b) Distinguish between combinational logic and sequential logic. [10+6]

8. (a) List the first 20 numbers in base17. Use the letters A, B, C, D, E, F and G to represent the last seven digits. [4]

(b) Convert the following numbers with the given radix to decimal.

i. 1234_5

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iv. 333_4 [3+3+3+3]

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Code No: R05210504 **R05** **Set No. 1**

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Time: 3 hours **Max Marks: 80**

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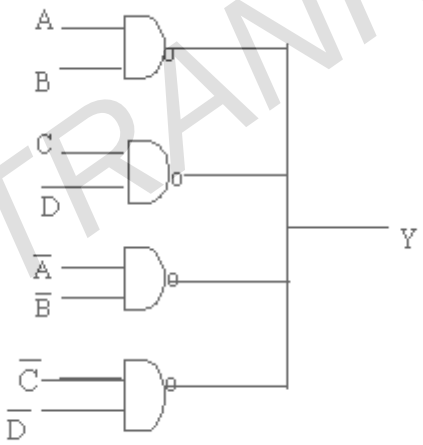

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   (b) A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are 1. The function is 0 otherwise. Write the HDL user - defined primitive for 3 bit majority functions. Assume A, B, C are the input variable and Y is the output variable. [8+8]

3. (a) Explain the concept of positive logic and negative logic. Also draw the truth tables for positive logic AND gate and negative logic OR gate.
   (b) Obtain the complement of the following Boolean expressions.
      i. B'C'D + (B + C + D)' + B'C'D'E
      ii. AB + (AC)' + (AB + C).
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4. (a) Using five lower - order demultiplexer, construct 6 to 64 line demultiplexer circuit. Use only block diagrams.

   (b) Design a Combinational logic circuit with three inputs A, B, C and three outputs x, y, z. If the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Draw the circuit using three-2 input AND gates, one 3 input OR gate, one 3 input X - OR gate and one inverter. [4+12]

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Code No: R05210504 **R05** **Set No. 1**

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Code No: R05210504 **R05** **Set No. 3**

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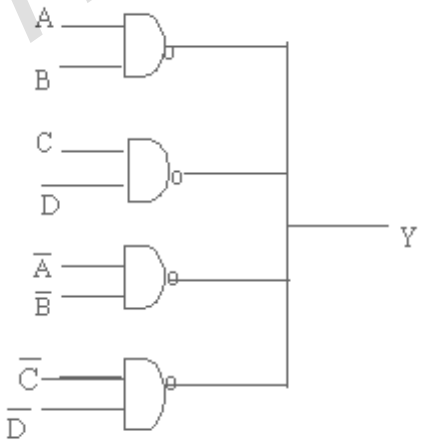

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