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Code No: R05220403 **R05** **Set No. 2**

II B.Tech II Semester Examinations,December 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input.
   (b) Write a brief note on programmable logic devices. [8+8]
2. (a) Compare synchronous & Asynchronous circuits
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]
3. Clocked sequential circuit with single input x and single output Z is described by the following J - K flip - flops. Input equations and output equations of Z
   $J_1 = Q_2 \quad K_1 = Q_2\overline{x}$
   $J_2 = \overline{x} \quad K_2 = x \oplus Q_1 \quad Z = (\overline{Q_1} + Q_2)x$
   (a) Draw the schematic circuit diagram.
   (b) Obtain state - table.
   (c) Obtain state diagram.
   (d) Obtain state equations. [4+4+4+4]
4. (a) Generate Hamming code for the given 11 bit message 10010110101 and rewrite the entire message with Hamming code. [8]
   (b) The binary numbers listed have a sign bit in the left most position and,if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. [4×2=8]
      i. 101011 + 111001
      ii. 001111 + 110010
      iii. 111001 - 011010
      iv. 101111 - 100110
5. (a) Simplify the following Boolean expressions. [8]
      i. A'C'+ABC+AC' to three literals
      ii. (x'y'+z)'+z+xy+wz to three literals
      iii. A'B(D'+C'D)+B(A+A'CD) to one literal
      iv. (A'+C)(A'+C')(A+B+C'D) to four literals
   (b) Obtain the complement of the following Boolean expressions. [8]

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i. B'C'D+(B+C+D)'+B'C'D'E
ii. AB+(AC)'+(AB+C)
iii. A'B'C'+A?BC'+AB'C'+ABC'
iv. AB+(AC)'+AB'C

6. (a) What is a cell of a K-map? What is meant by pair, a quad, and an octet of a map and how many variables are eliminated? [8]
   (b) Reduce the following function using K- map and implement it using NAND logic. F= $\sum m(0, 2, 3, 4, 5, 6,)$ [8]

7. For the ASM chart given 2:

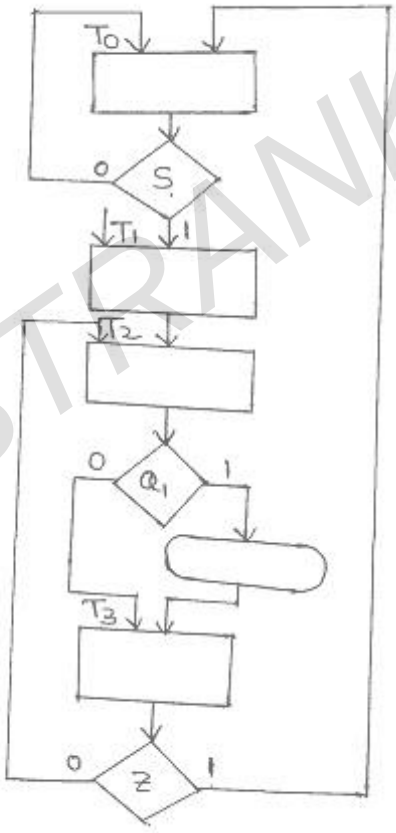

Figure 2

   (a) Draw the state diagram.
   (b) Design the control unit using D flip-flops and a decoder. [8+8]

8. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
   $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
   $Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
   $Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$

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(b) Explain the terms Multiplexing and Demultiplexing. [10+6]

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Code No: R05220403 **R05** **Set No. 4**

II B.Tech II Semester Examinations,December 2010
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Simplify the following Boolean expressions. [8]
   i. A'C'+ABC+AC' to three literals
   ii. (x'y'+z)'+z+xy+wz to three literals
   iii. A'B(D'+C'D)+B(A+A'CD) to one literal
   iv. (A'+C)(A'+C')(A+B+C'D) to four literals
   (b) Obtain the complement of the following Boolean expressions. [8]
   i. B'C'D+(B+C+D)'+B'C'D'E
   ii. AB+(AC)'+(AB+C)
   iii. A'B'C'+A?BC'+AB'C'+ABC'
   iv. AB+(AC)'+AB'C
2. For the ASM chart given 2:

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Code No: R05220403 **R05** **Set No. 4**

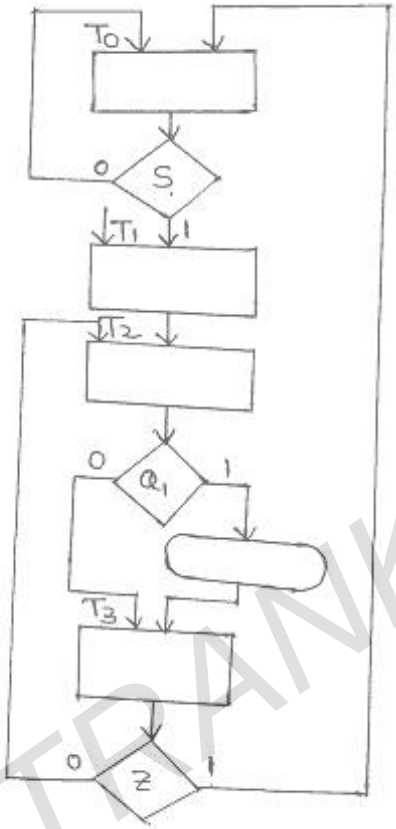

Figure 2

(a) Draw the state diagram.

(b) Design the control unit using D flip-flops and a decoder. [8+8]

3. (a) Compare synchronous & Asynchronous circuits

(b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

4. Clocked sequential circuit with single input x and single output Z is described by the following J - K flip - flops. Input equations and output equations of Z

$J_1 = Q_2 \quad K_1 = Q_2\overline{x}$

$J_2 = \overline{x} \quad K_2 = x \oplus Q_1 \quad Z = (\overline{Q_1} + Q_2)x$

(a) Draw the schematic circuit diagram.

(b) Obtain state - table.

(c) Obtain state diagram.

(d) Obtain state equations. [4+4+4+4]

5. (a) Generate Hamming code for the given 11 bit message 10010110101 and rewrite the entire message with Hamming code. [8]

(b) The binary numbers listed have a sign bit in the left most position and,if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. [4×2=8]

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i. 101011 + 111001
ii. 001111 + 110010
iii. 111001 - 011010
iv. 101111 - 100110

6. (a) What is a cell of a K-map? What is meant by pair, a quad, and an octet of a map and how many variables are eliminated? [8]
   (b) Reduce the following function using K- map and implement it using NAND logic. F= $\sum m(0, 2, 3, 4, 5, 6,)$ [8]

7. (a) Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input.
   (b) Write a brief note on programmable logic devices. [8+8]

8. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
   $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD$
   $Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
   $Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$
   (b) Explain the terms Multiplexing and Demultiplexing. [10+6]

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Code No: R05220403 **R05** **Set No. 1**

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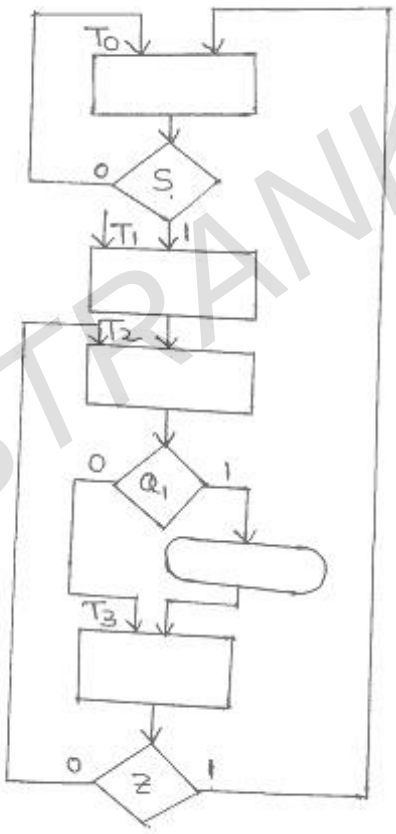

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Figure 2

(a) Draw the state diagram.

(b) Design the control unit using D flip-flops and a decoder. [8+8]

2. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
$Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
$Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
$Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$

(b) Explain the terms Multiplexing and Demultiplexing. [10+6]

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Code No: R05220403 **R05** **Set No. 1**

3. (a) Simplify the following Boolean expressions. [8]
   i. A'C'+ABC+AC' to three literals
   ii. (x'y'+z)'+z+xy+wz to three literals
   iii. A'B(D'+C'D)+B(A+A'CD) to one literal
   iv. (A'+C)(A'+C')(A+B+C'D) to four literals
   (b) Obtain the complement of the following Boolean expressions. [8]
   i. B'C'D+(B+C+D)'+B'C'D'E
   ii. AB+(AC)'+(AB+C)
   iii. A'B'C'+A?BC'+AB'C'+ABC'
   iv. AB+(AC)'+AB'C

4. (a) Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input.
   (b) Write a brief note on programmable logic devices. [8+8]

5. (a) What is a cell of a K-map? What is meant by pair, a quad, and an octet of a map and how many variables are eliminated? [8]
   (b) Reduce the following function using K- map and implement it using NAND logic. F= $\sum m(0, 2, 3, 4, 5, 6,)$ [8]

6. (a) Generate Hamming code for the given 11 bit message 10010110101 and rewrite the entire message with Hamming code. [8]
   (b) The binary numbers listed have a sign bit in the left most position and,if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. [4×2=8]
   i. 101011 + 111001
   ii. 001111 + 110010
   iii. 111001 - 011010
   iv. 101111 - 100110

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   $J_1 = Q_2$ $K_1 = Q_2\overline{x}$
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   (a) Draw the schematic circuit diagram.
   (b) Obtain state - table.
   (c) Obtain state diagram.
   (d) Obtain state equations. [4+4+4+4]

8. (a) Compare synchronous & Asynchronous circuits
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

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Code No: R05220403 **R05** **Set No. 3**

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Time: 3 hours **Max Marks: 80**

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1. (a) Compare synchronous & Asynchronous circuits
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

2. For the ASM chart given 2:

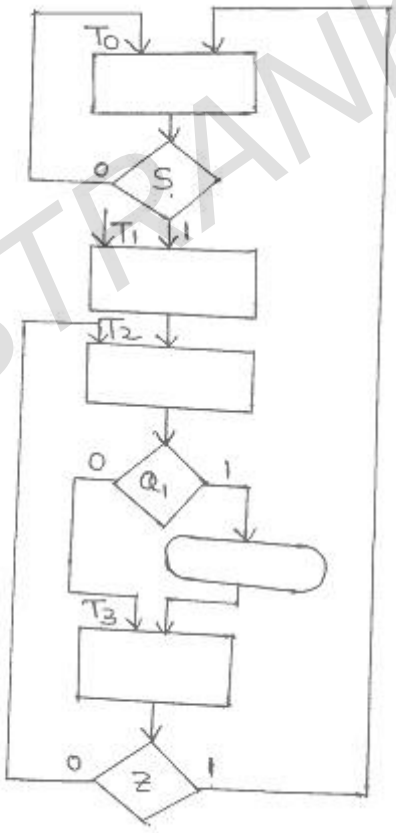

Figure 2

   (a) Draw the state diagram.
   (b) Design the control unit using D flip-flops and a decoder. [8+8]

3. (a) Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input.
   (b) Write a brief note on programmable logic devices. [8+8]

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4. (a) Simplify the following Boolean expressions. [8]
   i. A'C'+ABC+AC' to three literals
   ii. (x'y'+z)'+z+xy+wz to three literals
   iii. A'B(D'+C'D)+B(A+A'CD) to one literal
   iv. (A'+C)(A'+C')(A+B+C'D) to four literals
   (b) Obtain the complement of the following Boolean expressions. [8]
   i. B'C'D+(B+C+D)'+B'C'D'E
   ii. AB+(AC)'+(AB+C)
   iii. A'B'C'+A?BC'+AB'C'+ABC'
   iv. AB+(AC)'+AB'C

5. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
   $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
   $Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
   $Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$
   (b) Explain the terms Multiplexing and Demultiplexing. [10+6]

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