Code No: R05311403 **R05** **Set No. 2**

III B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Mechatronics

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Design a clocked sequential circuit for the state diagram shown in figure 1a

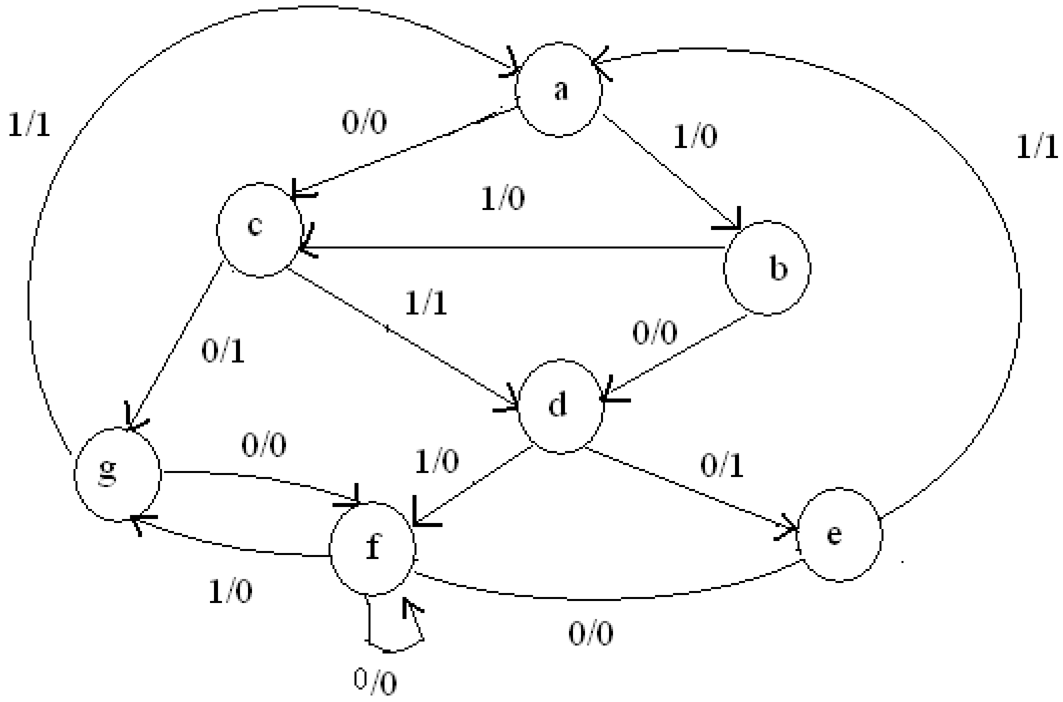

Figure 1a

(b) Explain about the following:

i. Shift counters

ii. Gray code counter. [8+8]

2. Reduce the following function using K-map,
F= $\prod M(1, 3, 4, 5, 6, 9, 11, 12, 14, 15, 17, 19, 20, 21, 23, 25, 27, 28, 30, 33, 35, 36, 38, 41, 43, 44, 46, 49, 51, 52, 54, 57, 59, 60, 62)$. [16]

3. A Clocked sequential circuit with single input x and single output Z is described by the following T - flip - flop. Input equations and output equations of Z .
$T_1 = \overline{Q_1}Q_2 + Q_2\overline{x}$
$T_2 = Q_1\overline{x} + \overline{Q_2}\overline{x} + \overline{Q_1}Q_2x$
$Z = (\overline{Q_1} + Q_2)x$

(a) Draw the schematic logic circuit.

(b) Obtain state - table.

(c) Obtain state - diagram.

(d) Obtain state - equations. [4+4+4+4]

4. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

   (b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

5. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
   $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
   $Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
   $Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$

   (b) Explain the terms Multiplexing and Demultiplexing. [10+6]

6. (a) Reduce the following Boolean expressions. [8]
   i. B'C'D+(B+C+D)'+B'C'D'E
   ii. AB+(AC)'+AB'C(AB+C)
   iii. A'B'C'+A'BC'+AB'C'+ABC'
   iv. A+B+A'B'C

   (b) Obtain the complement of the following Boolean expressions. [8]
   i. x'y'+xy+x'y
   ii. xy'+y'z'+x'z'
   iii. x+xy+xz'+xy'z'
   iv. (x+y)(x+y')

7. For the state diagram given 7:

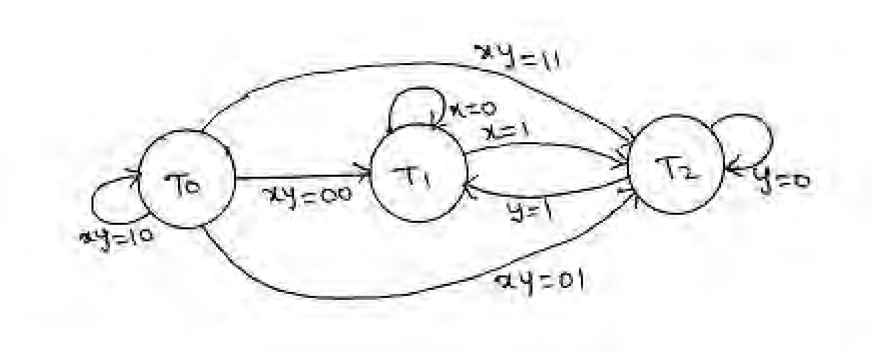

Figure 7

(a) Draw the equivalent ASM chart.

(b) Design the control circuit using one Flip-Flop per state method. [8+8]

8. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows. [4 ×4 = 16]

   (a) 000011101010
   (b) 101110000110
   (c) 101111110100
   (d) 110011010010

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Code No: R05311403 **R05** **Set No. 4**

III B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

   (b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

2. Reduce the following function using K-map,
   F= $\prod M(1, 3, 4, 5, 6, 9, 11, 12, 14, 15, 17, 19, 20, 21, 23, 25, 27, 28, 30, 33, 35, 36, 38, 41, 43, 44, 46, 49, 51, 52, 54, 57, 59, 60, 62)$. [16]

3. (a) Reduce the following Boolean expressions. [8]

      i. B'C'D+(B+C+D)'+B'C'D'E
      ii. AB+(AC)'+AB'C(AB+C)
      iii. A'B'C'+A'BC'+AB'C'+ABC'
      iv. A+B+A'B'C

   (b) Obtain the complement of the following Boolean expressions. [8]

      i. x'y'+xy+x'y
      ii. xy'+y'z'+x'z'
      iii. x+xy+xz'+xy'z'
      iv. (x+y)(x+y')

4. (a) Design a clocked sequential circuit for the state diagram shown in figure 4a

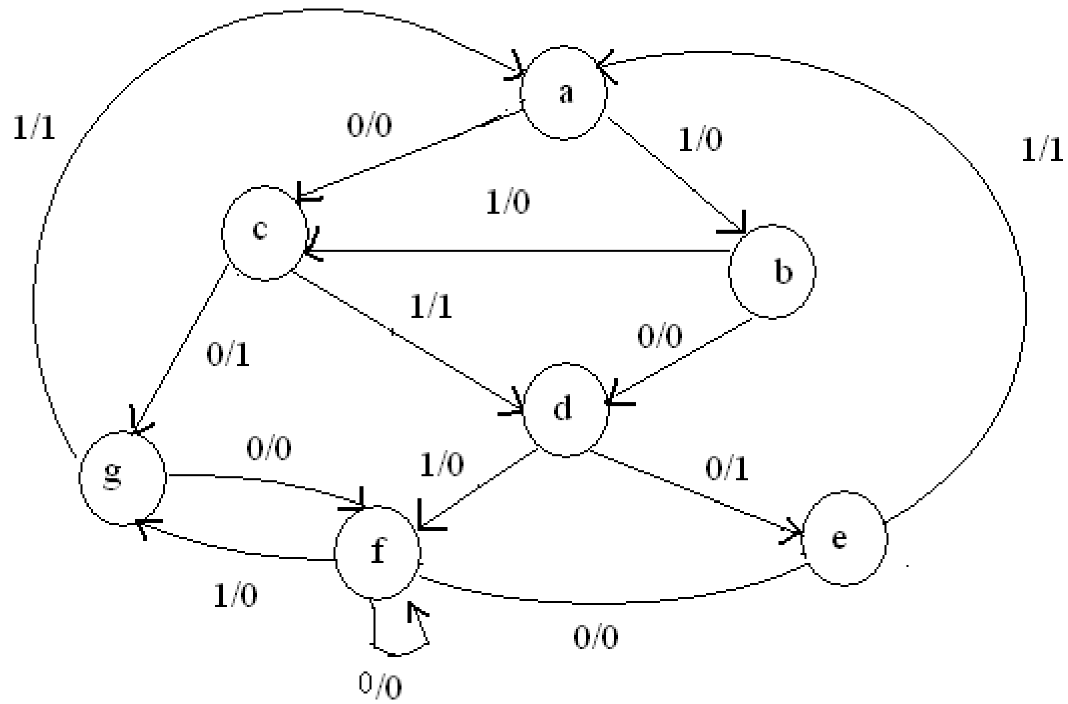

Figure 4a

(b) Explain about the following:

i. Shift counters

ii. Gray code counter. [8+8]

5. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
$Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
$Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
$Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$

(b) Explain the terms Multiplexing and Demultiplexing. [10+6]

6. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows. [4 ×4 = 16]

(a) 000011101010

(b) 101110000110

(c) 101111110100

(d) 110011010010

7. For the state diagram given 7:

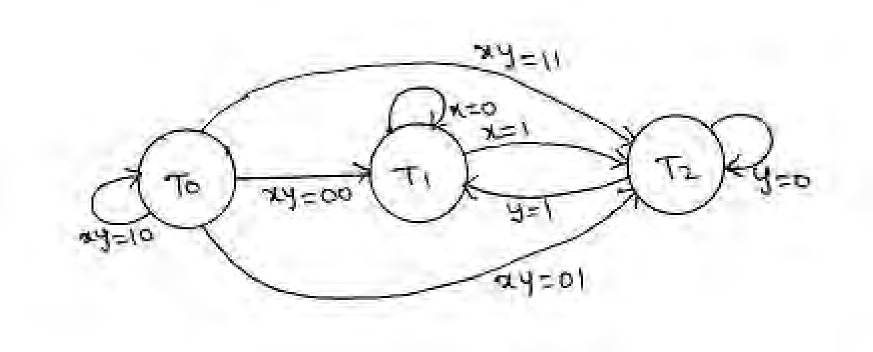

Figure 7

(a) Draw the equivalent ASM chart.

(b) Design the control circuit using one Flip-Flop per state method. [8+8]

8. A Clocked sequential circuit with single input x and single output Z is described by the following T - flip - flop. Input equations and output equations of Z .
$T_1 = \overline{Q_1}Q_2 + Q_2\overline{x}$
$T_2 = Q_1\overline{x} + \overline{Q_2}\overline{x} + \overline{Q_1}Q_2x$
$Z = (\overline{Q_1} + Q_2)x$

(a) Draw the schematic logic circuit.

(b) Obtain state - table.

(c) Obtain state - diagram.

(d) Obtain state - equations. [4+4+4+4]

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Code No: R05311403 **R05** **Set No. 1**

III B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Reduce the following function using K-map,
F= $\prod M(1, 3, 4, 5, 6, 9, 11, 12, 14, 15, 17, 19, 20, 21, 23, 25, 27, 28, 30, 33, 35, 36, 38, 41, 43, 44, 46, 49, 51, 52, 54, 57, 59, 60, 62)$. [16]

2. (a) Design a clocked sequential circuit for the state diagram shown in figure 2a

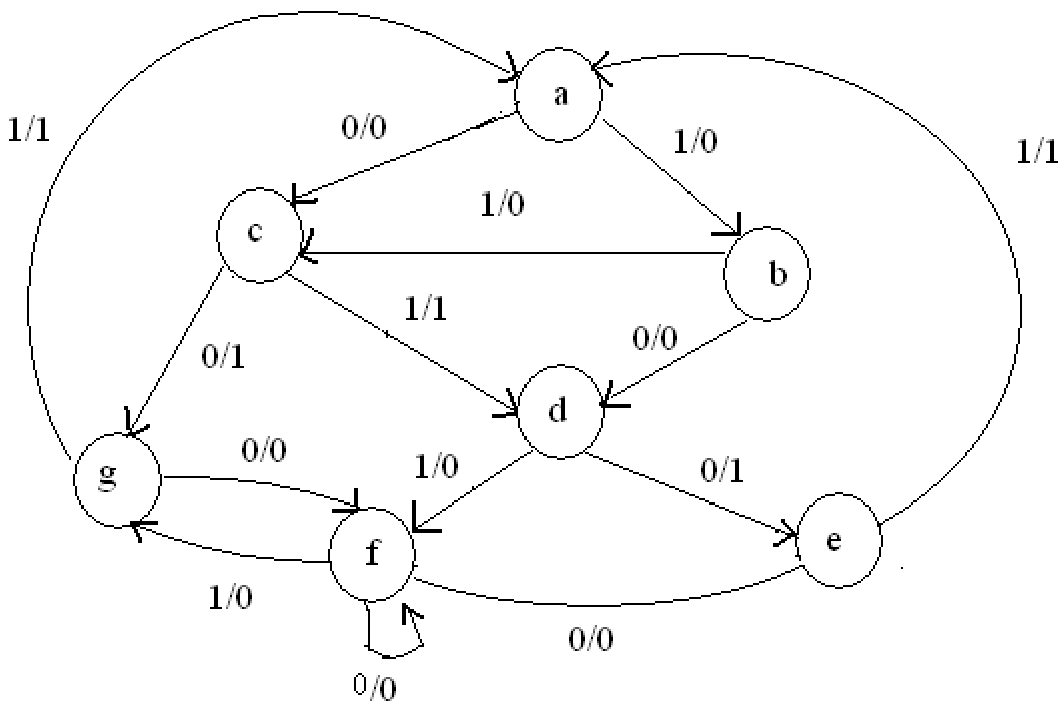

Figure 2a

(b) Explain about the following:

i. Shift counters
ii. Gray code counter. [8+8]

3. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

(b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Code No: R05311403 **R05** **Set No. 1**

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

4. (a) Reduce the following Boolean expressions. [8]
   i. B'C'D+(B+C+D)'+B'C'D'E
   ii. AB+(AC)'+AB'C(AB+C)
   iii. A'B'C'+A'BC'+AB'C'+ABC'
   iv. A+B+A'B'C

   (b) Obtain the complement of the following Boolean expressions. [8]
   i. x'y'+xy+x'y
   ii. xy'+y'z'+x'z'
   iii. x+xy+xz'+xy'z'
   iv. (x+y)(x+y')

5. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows. [4 ×4 = 16]
   (a) 000011101010
   (b) 101110000110
   (c) 101111110100
   (d) 110011010010

6. For the state diagram given 6:

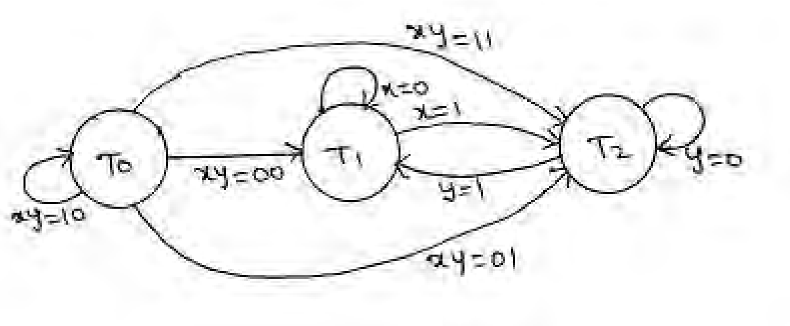

Figure 6

   (a) Draw the equivalent ASM chart.

(b) Design the control circuit using one Flip-Flop per state method. [8+8]

7. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
$Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
$Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
$Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$

(b) Explain the terms Multiplexing and Demultiplexing. [10+6]

8. A Clocked sequential circuit with single input x and single output Z is described by the following T - flip - flop. Input equations and output equations of Z .
$T_1 = \overline{Q_1}Q_2 + Q_2\overline{x}$
$T_2 = Q_1\overline{x} + \overline{Q_2}\overline{x} + \overline{Q_1}Q_2x$
$Z = (\overline{Q_1} + Q_2)x$

(a) Draw the schematic logic circuit.
(b) Obtain state - table.
(c) Obtain state - diagram.
(d) Obtain state - equations. [4+4+4+4]

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Code No: R05311403 **R05** **Set No. 3**

III B.Tech I Semester Examinations,November 2010
SWITCHING THEORY AND LOGIC DESIGN
Mechatronics

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. For the state diagram given 1:

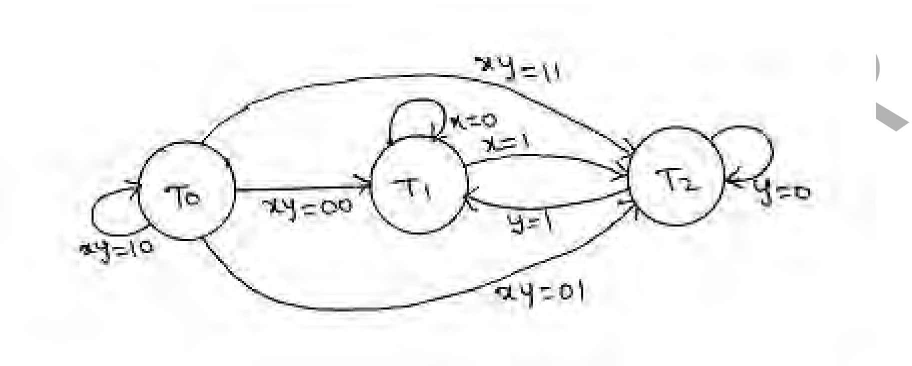

Figure 1

   (a) Draw the equivalent ASM chart.
   (b) Design the control circuit using one Flip-Flop per state method. [8+8]

2. Reduce the following function using K-map,
   F= $\prod M(1, 3, 4, 5, 6, 9, 11, 12, 14, 15, 17, 19, 20, 21, 23, 25, 27, 28, 30, 33, 35, 36, 38, 41, 43, 44, 46, 49, 51, 52, 54, 57, 59, 60, 62)$. [16]

3. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
   $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
   $Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
   $Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$
   (b) Explain the terms Multiplexing and Demultiplexing. [10+6]

4. (a) Reduce the following Boolean expressions. [8]
      i. B'C'D+(B+C+D)'+B'C'D'E
      ii. AB+(AC)'+AB'C(AB+C)
      iii. A'B'C'+A'BC'+AB'C'+ABC'
      iv. A+B+A'B'C
   (b) Obtain the complement of the following Boolean expressions. [8]
      i. x'y'+xy+x'y
      ii. xy'+y'z'+x'z'
      iii. x+xy+xz'+xy'z'

iv. (x+y)(x+y')

5. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows. [4 ×4 = 16]

   (a) 000011101010
   (b) 101110000110
   (c) 101111110100
   (d) 110011010010

6. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

   (b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

7. (a) Design a clocked sequential circuit for the state diagram shown in figure 7a

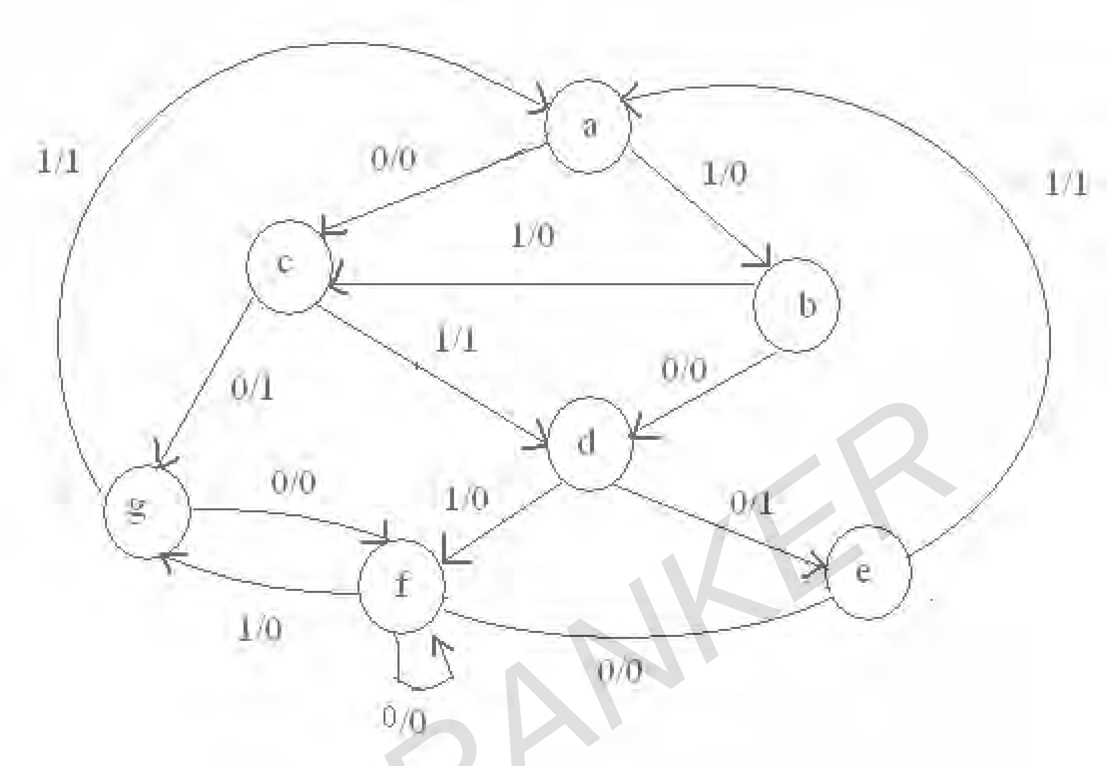

Figure 7a

(b) Explain about the following:

i. Shift counters

ii. Gray code counter. [8+8]

8. A Clocked sequential circuit with single input x and single output Z is described by the following T - flip - flop. Input equations and output equations of Z .
$T_1 = \overline{Q_1}Q_2 + Q_2\overline{x}$
$T_2 = Q_1\overline{x} + \overline{Q_2}\overline{x} + \overline{Q_1}Q_2x$
$Z = (\overline{Q_1} + Q_2)x$

(a) Draw the schematic logic circuit.

(b) Obtain state - table.

(c) Obtain state - diagram.

(d) Obtain state - equations. [4+4+4+4]

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