Code No: R05320402 **R05** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) How to represent a tristate in VHDL and explain it with suitable program.
   (b) What is rat's-nest wiring diagram? Explain its significance in system design. [8+8]

2. (a) Draw and explain the FPGA chip architecture.
   (b) Draw and explain the AND/NOR representation of PLA. [8+8]

3. (a) Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram and layout.
   (b) Draw a schematic for a CMOS edge-sensitive scan-register and also draw some circuit level diagrams of its implementation. [8+8]

4. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]

5. Calculate the ON resistance of the circuit shown in the figure 7 from V_{DD} to GND. If n- channel sheet resistance $R_{sn} = 10^4\ \Omega$ per square and P-channel sheet resistance $R_{sp} = 2.5 \times 10^4\ \Omega$ per square. [16]

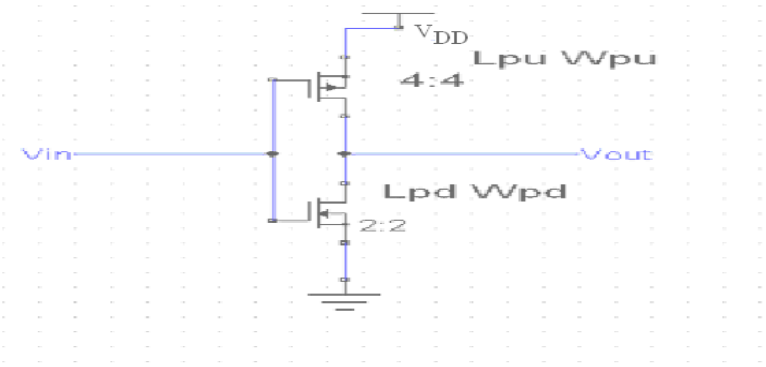

Figure 7

6. (a) Explain CMOS P - well fabrication process steps with neat sketches.
   (b) Draw and explian the cross sectional view of N- well CMOS inverter. [8+8]

7. (a) Calculate body factor of threshold for the given parameters N_A =$3 \times 10^{16} cm^{-3}$, $t_{ox} = 200A^0$, ε_{ox} =$3.9 \times 8.85 \times 10-14$ F/cm, ε_{si}=$11.7 \times 8.85 \times 10-14$F/cm, Electron charge =$1.6 \times 10^{-19}$ coulombs.

(b) Mention the parameters on which the threshold voltage depends. [8+8]

8. (a) Draw and explain the layout for a combinational adder appropriate for a data path.

(b) Draw the Serial/parallel multiplier structure and explain how multiplication is performed. [8+8]

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Code No: R05320402 **R05** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]

2. Calculate the ON resistance of the circuit shown in the figure 7 from V_{DD} to GND. If n- channel sheet resistance $R_{sn} = 10^4\ \Omega$ per square and P-channel sheet resistance $R_{sp} = 2.5 \times 10^4\ \Omega$ per square. [16]

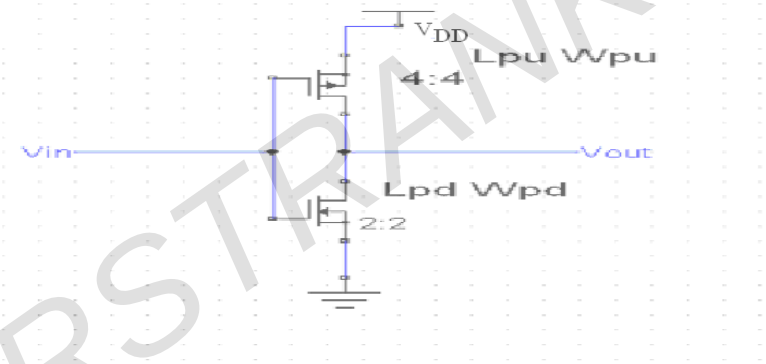

Figure 7

3. (a) Draw and explain the FPGA chip architecture.
   (b) Draw and explain the AND/NOR representation of PLA. [8+8]

4. (a) How to represent a tristate in VHDL and explain it with suitable program.
   (b) What is rat's-nest wiring diagram? Explain its significance in system design. [8+8]

5. (a) Calculate body factor of threshold for the given parameters N_A =$3 \times 10^{16} cm^{-3}$, $t_{ox} = 200A^0$, ε_{ox} =$3.9 \times 8.85 \times 10-14$ F/cm, ε_{si}=$11.7 \times 8.85 \times 10-14$F/cm, Electron charge =$1.6 \times 10^{-19}$ coulombs.
   (b) Mention the parameters on which the threshold voltage depends. [8+8]

6. (a) Explain CMOS P - well fabrication process steps with neat sketches.
   (b) Draw and explian the cross sectional view of N- well CMOS inverter. [8+8]

7. (a) Draw and explain the layout for a combinational adder appropriate for a data path.
   (b) Draw the Serial/parallel multiplier structure and explain how multiplication is performed. [8+8]

8. (a) Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram and layout.

   (b) Draw a schematic for a CMOS edge-sensitive scan-register and also draw some circuit level diagrams of its implementation. [8+8]

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Code No: R05320402 **R05** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw and explain the FPGA chip architecture.
   (b) Draw and explain the AND/NOR representation of PLA. [8+8]

2. Calculate the ON resistance of the circuit shown in the figure 7 from V_{DD} to GND. If n- channel sheet resistance $R_{sn} = 10^4\ \Omega$ per square and P-channel sheet resistance $R_{sp} = 2.5 \times 10^4\ \Omega$ per square. [16]

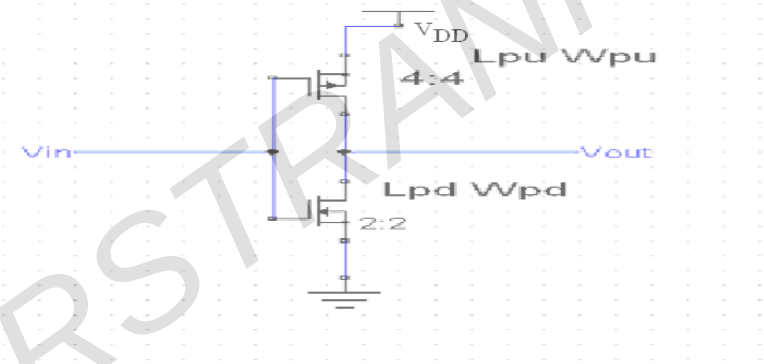

Figure 7

3. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]

4. (a) How to represent a tristate in VHDL and explain it with suitable program.
   (b) What is rat's-nest wiring diagram? Explain its significance in system design. [8+8]

5. (a) Explain CMOS P - well fabrication process steps with neat sketches.
   (b) Draw and explian the cross sectional view of N- well CMOS inverter. [8+8]

6. (a) Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram and layout.
   (b) Draw a schematic for a CMOS edge-sensitive scan-register and also draw some circuit level diagrams of its implementation. [8+8]

7. (a) Calculate body factor of threshold for the given parameters N_A =3 $\times$ $10^{16} cm^{-3}$, $t_{ox} = 200A^0$, ε_{ox} =3.9 $\times$ 8.85 $\times$ 10−14 F/cm, ε_{si}=11.7 $\times$ 8.85 $\times$ 10−14F/cm, Electron charge =1.6 $\times$ 10^{-19} coulombs.

(b) Mention the parameters on which the threshold voltage depends. [8+8]

8. (a) Draw and explain the layout for a combinational adder appropriate for a data path.

(b) Draw the Serial/parallel multiplier structure and explain how multiplication is performed. [8+8]

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Code No: R05320402 **R05** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
VLSI DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) How to represent a tristate in VHDL and explain it with suitable program.
   (b) What is rat's-nest wiring diagram? Explain its significance in system design. [8+8]
2. (a) Draw and explain the FPGA chip architecture.
   (b) Draw and explain the AND/NOR representation of PLA. [8+8]
3. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]
4. (a) Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram and layout.
   (b) Draw a schematic for a CMOS edge-sensitive scan-register and also draw some circuit level diagrams of its implementation. [8+8]
5. (a) Explain CMOS P - well fabrication process steps with neat sketches.
   (b) Draw and explian the cross sectional view of N- well CMOS inverter. [8+8]
6. (a) Draw and explain the layout for a combinational adder appropriate for a data path.
   (b) Draw the Serial/parallel multiplier structure and explain how multiplication is performed. [8+8]
7. Calculate the ON resistance of the circuit shown in the figure 7 from V_{DD} to GND. If n- channel sheet resistance $R_{sn} = 10^4\ \Omega$ per square and P-channel sheet resistance $R_{sp} = 2.5 \times 10^4\ \Omega$ per square. [16]

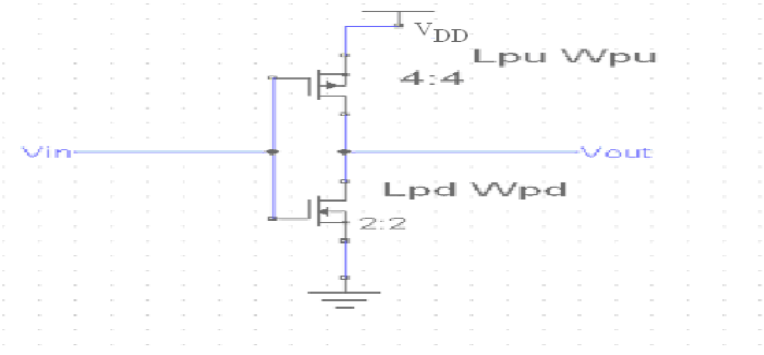

Figure 7

8. (a) Calculate body factor of threshold for the given parameters
N_A =$3 \times 10^{16} cm^{-3}$, $t_{ox} = 200A^0$, ε_{ox} =$3.9 \times 8.85 \times 10-14$ F/cm,
ε_{si}=$11.7 \times 8.85 \times 10-14$F/cm, Electron charge =$1.6 \times 10^{-19}$ coulombs.

   (b) Mention the parameters on which the threshold voltage depends. [8+8]

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