Code No: R05321405 **R05** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
   (b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms:
      i. FIFO
      ii. LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. [8+8]
2. (a) What are the major design considerations in microinstruction sequencing? [8]
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. [8]
3. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]
4. What are the different modes of data transfer? Explain each mode in detail. [16]
5. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]
6. Draw circuit for BCD addition and subtraction. Explain its functionality with mathematical background. [16]
7. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck?. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]
8. Design a circuit with half adder units to increment or decrement the content of a 4-bit register with RS flip-flops. [16]

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Code No: R05321405 **R05** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the major design considerations in microinstruction sequencing? [8]
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. [8]
2. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
   (b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms:
      i. FIFO
      ii. LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. [8+8]
3. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]
4. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck?. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]
5. What are the different modes of data transfer? Explain each mode in detail. [16]
6. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]
7. Design a circuit with half adder units to increment or decrement the content of a 4-bit register with RS flip-flops. [16]
8. Draw circuit for BCD addition and subtraction. Explain its functionality with mathematical background. [16]

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Code No: R05321405 **R05** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]
2. (a) What are the major design considerations in microinstruction sequencing? [8]
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. [8]
3. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
   (b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms:
      i. FIFO
      ii. LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. [8+8]
4. Design a circuit with half adder units to increment or decrement the content of a 4-bit register with RS flip-flops. [16]
5. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck?. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]
6. What are the different modes of data transfer? Explain each mode in detail. [16]
7. Draw circuit for BCD addition and subtraction. Explain its functionality with mathematical background. [16]
8. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]

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Code No: R05321405 **R05** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]
2. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]
3. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
   (b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms:
      i. FIFO
      ii. LRU if the reference string is as follows:
      4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. [8+8]
4. Draw circuit for BCD addition and subtraction. Explain its functionality with mathematical background. [16]
5. (a) What are the major design considerations in microinstruction sequencing? [8]
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. [8]
6. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck?. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]
7. What are the different modes of data transfer? Explain each mode in detail. [16]
8. Design a circuit with half adder units to increment or decrement the content of a 4-bit register with RS flip-flops. [16]

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