Code No: RR320202 **RR** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND INTERFACING
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [8+8]
2. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]
3. (a) Discuss the sequence of operations performed in the interrupt acknowledge cycle?
   (b) What is the purpose of IF flag in handling the interrupts?
   (c) Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? [5+5+6]
4. (a) What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions. [8]
   (b) Give the assembly language implementation of the following.
      i. IF-THAN-ELSE
      ii. REPEAT [4+4]
5. (a) How does 8051 differentiate between the external and internal program memory?
   (b) Explain how serial data communication is done with 8051 ports? [6+10]
6. (a) What is the use of trap flag? Discuss how trap flag provides debugging feature?
   (b) What is the difference between physical address, effective address and offset address? Explain with example how physical address is generated? [7+9]
7. (a) Distinguish between synchronous and asynchronous serial data transmission techniques? Discuss the advantages and disadvantages? [8]
   (b) Draw the block diagram of combination of FAX and Data Modem? Explain each block? [4+4]

8. The I/O circuitry in an 8086 based system consists of five I/O devices with one status signal for each device. Design the required hardware providing two address locations to each device, one for status and other for data. In the range 0F00H to 0FOFH. Write an instruction sequence to test the status of each device and store it. [16]

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Code No: RR320202 **RR** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND INTERFACING
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is the use of trap flag? Discuss how trap flag provides debugging feature?
   (b) What is the difference between physical address, effective address and offset address? Explain with example how physical address is generated? [7+9]

2. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]

3. (a) What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions. [8]
   (b) Give the assembly language implementation of the following.
      i. IF-THAN-ELSE
      ii. REPEAT [4+4]

4. (a) Distinguish between synchronous and asynchronous serial data transmission techniques? Discuss the advantages and disadvantages? [8]
   (b) Draw the block diagram of combination of FAX and Data Modem? Explain each block? [4+4]

5. The I/O circuitry in an 8086 based system consists of five I/O devices with one status signal for each device. Design the required hardware providing two address locations to each device, one for status and other for data. In the range 0F00H to 0FOFH. Write an instruction sequence to test the status of each device and store it. [16]

6. (a) Discuss the sequence of operations performed in the interrupt acknowledge cycle?
   (b) What is the purpose of IF flag in handling the interrupts?
   (c) Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? [5+5+6]

7. (a) How does 8051 differentiate between the external and internal program memory?
   (b) Explain how serial data communication is done with 8051 ports? [6+10]

8. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [8+8]

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Code No: RR320202 **RR** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND INTERFACING
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]

2. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [8+8]

3. The I/O circuitry in an 8086 based system consists of five I/O devices with one status signal for each device. Design the required hardware providing two address locations to each device, one for status and other for data. In the range 0F00H to 0FOFH. Write an instruction sequence to test the status of each device and store it. [16]

4. (a) How does 8051 differentiate between the external and internal program memory?
   (b) Explain how serial data communication is done with 8051 ports? [6+10]

5. (a) What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions. [8]
   (b) Give the assembly language implementation of the following.
      i. IF-THAN-ELSE
      ii. REPEAT [4+4]

6. (a) Distinguish between synchronous and asynchronous serial data transmission techniques? Discuss the advantages and disadvantages? [8]
   (b) Draw the block diagram of combination of FAX and Data Modem? Explain each block? [4+4]

7. (a) Discuss the sequence of operations performed in the interrupt acknowledge cycle?
   (b) What is the purpose of IF flag in handling the interrupts?
   (c) Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? [5+5+6]

8. (a) What is the use of trap flag? Discuss how trap flag provides debugging feature?
   (b) What is the difference between physical address, effective address and offset address? Explain with example how physical address is generated? [7+9]

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Code No: RR320202 **RR** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND INTERFACING
Common to BME, ETM, E.CONT.E, EIE, ECE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is the use of trap flag? Discuss how trap flag provides debugging feature?
   (b) What is the difference between physical address, effective address and offset address? Explain with example how physical address is generated? [7+9]
2. (a) Distinguish between synchronous and asynchronous serial data transmission techniques? Discuss the advantages and disadvantages? [8]
   (b) Draw the block diagram of combination of FAX and Data Modem? Explain each block? [4+4]
3. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [8+8]
4. (a) What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions. [8]
   (b) Give the assembly language implementation of the following.
      i. IF-THAN-ELSE
      ii. REPEAT [4+4]
5. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]
6. (a) How does 8051 differentiate between the external and internal program memory?
   (b) Explain how serial data communication is done with 8051 ports? [6+10]
7. The I/O circuitry in an 8086 based system consists of five I/O devices with one status signal for each device. Design the required hardware providing two address locations to each device, one for status and other for data. In the range 0F00H to 0FOFH. Write an instruction sequence to test the status of each device and store it. [16]
8. (a) Discuss the sequence of operations performed in the interrupt acknowledge cycle?

(b) What is the purpose of IF flag in handling the interrupts?

(c) Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? [5+5+6]

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