Code No: RR321202 **RR** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
VLSI SYSTEMS DESIGN
Information Technology

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Implement EX-OR and EX-NOR gates using static complementary logic. [16]
2. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models [16]
3. Draw the Architecture of PLA and explain how different logic functions can be implemented using PLA. [16]
4. Design the seven segment decoding function :
   Write a truth table whose rows are the digits 0 - 9 and whose columns are the on signals for the seven segments. [16]
5. Explain about the following
   (a) Why is n diff - to - p diff spacing so large.
   (b) Why is metal - metal spacing larger than poly - poly spacing
   (c) Why is metal 2 - metal2 spacing larger than metal1 - metal1 spacing[6+5+5]
6. Explain about the data - path controller architecture of register transfer machine. [16]
7. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input OR gate.
   (b) 4 Input NAND gate. [8+8]
8. (a) Define the terms Analog systems & Digital system with Two Examples.
   (b) Define the terms logic family, Saturated logic and non-saturated logic [8+8]

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Code No: RR321202 **RR** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
VLSI SYSTEMS DESIGN
Information Technology

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain about the following
   (a) Why is n diff - to - p diff spacing so large.
   (b) Why is metal - metal spacing larger than poly - poly spacing
   (c) Why is metal 2 - metal2 spacing larger than metal1 - metal1 spacing[6+5+5]
2. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input OR gate.
   (b) 4 Input NAND gate. [8+8]
3. Implement EX-OR and EX-NOR gates using static complementary logic. [16]
4. Design the seven segment decoding function :
   Write a truth table whose rows are the digits 0 - 9 and whose columns are the on signals for the seven segments. [16]
5. Draw the Architecture of PLA and explain how different logic functions can be implemented using PLA. [16]
6. (a) Define the terms Analog systems & Digital system with Two Examples.
   (b) Define the terms logic family, Saturated logic and non-saturated logic [8+8]
7. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models [16]
8. Explain about the data - path controller architecture of register transfer machine. [16]

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Code No: RR321202 **RR** **Set No. 1**

III B.Tech II Semester Examinations,December 2010
VLSI SYSTEMS DESIGN
Information Technology

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement EX-OR and EX-NOR gates using static complementary logic. [16]
2. Design the seven segment decoding function :
   Write a truth table whose rows are the digits 0 - 9 and whose columns are the on signals for the seven segments. [16]
3. Explain about the following
   (a) Why is n diff - to - p diff spacing so large.
   (b) Why is metal - metal spacing larger than poly - poly spacing
   (c) Why is metal 2 - metal2 spacing larger than metal1 - metal1 spacing[6+5+5]
4. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models [16]
5. (a) Define the terms Analog systems & Digital system with Two Examples.
   (b) Define the terms logic family, Saturated logic and non-saturated logic [8+8]
6. Explain about the data - path controller architecture of register transfer machine. [16]
7. Draw the Architecture of PLA and explain how different logic functions can be implemented using PLA. [16]
8. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input OR gate.
   (b) 4 Input NAND gate. [8+8]

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Code No: RR321202 **RR** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
VLSI SYSTEMS DESIGN
Information Technology

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input OR gate.
   (b) 4 Input NAND gate. [8+8]
2. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models [16]
3. (a) Define the terms Analog systems & Digital system with Two Examples.
   (b) Define the terms logic family, Saturated logic and non-saturated logic [8+8]
4. Draw the Architecture of PLA and explain how different logic functions can be implemented using PLA. [16]
5. Explain about the data - path controller architecture of register transfer machine. [16]
6. Design the seven segment decoding function :
   Write a truth table whose rows are the digits 0 - 9 and whose columns are the on signals for the seven segments. [16]
7. Explain about the following
   (a) Why is n diff - to - p diff spacing so large.
   (b) Why is metal - metal spacing larger than poly - poly spacing
   (c) Why is metal 2 - metal2 spacing larger than metal1 - metal1 spacing[6+5+5]
8. Implement EX-OR and EX-NOR gates using static complementary logic. [16]

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