Code No: RR322203 **RR** **Set No. 2**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO CONTROLLERS
Instrumentation And Control Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss the system bus cycle of 8086 with a neat diagram? What is the use of wait cycles? Compare wait and idle cycles?
   (b) Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086? [8+8]
2. (a) Discuss the organization of FLASH memory? Explain FLASH memory command definitions?
   (b) Why do you need wait states? Explain how wait states are generated?
   (c) Give possible solutions to meet the processor access time requirements when memory is interfaced to the processor? [7+4+5]
3. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?
   (b) Explain single transfer mode and block transfer mode of 8237? [8+8]
4. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? [8+8]
5. (a) Using DF flag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions.
   (b) Discuss the importance of procedures in assembly language programming? [10+6]
6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7?
   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]
7. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.

(a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.

(b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.

(c) Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.

(d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]

8. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?

(a) PCON

(b) PSW

(c) IP

(d) TMOD [4x4=16]

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Code No: RR322203 **RR** **Set No. 4**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO CONTROLLERS
Instrumentation And Control Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?
   (b) Explain single transfer mode and block transfer mode of 8237? [8+8]
2. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
   (a) PCON
   (b) PSW
   (c) IP
   (d) TMOD [4x4=16]
3. (a) Using DF flag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions.
   (b) Discuss the importance of procedures in assembly language programming? [10+6]
4. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? [8+8]
5. (a) Discuss the organization of FLASH memory? Explain FLASH memory command definitions?
   (b) Why do you need wait states? Explain how wait states are generated?
   (c) Give possible solutions to meet the processor access time requirements when memory is interfaced to the processor? [7+4+5]
6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7?
   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]

7. (a) Discuss the system bus cycle of 8086 with a neat diagram? What is the use of wait cycles? Compare wait and idle cycles?

   (b) Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086? [8+8]

8. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.

   (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.

   (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.

   (c) Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.

   (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]

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Code No: RR322203 **RR** **Set No. 1**

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MICROPROCESSORS AND MICRO CONTROLLERS
Instrumentation And Control Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss the organization of FLASH memory? Explain FLASH memory command definitions?
   (b) Why do you need wait states? Explain how wait states are generated?
   (c) Give possible solutions to meet the processor access time requirements when memory is interfaced to the processor? [7+4+5]
2. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
   (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
   (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
   (c) Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
   (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]
3. (a) Discuss the system bus cycle of 8086 with a neat diagram? What is the use of wait cycles? Compare wait and idle cycles?
   (b) Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086? [8+8]
4. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?
   (b) Explain single transfer mode and block transfer mode of 8237? [8+8]
5. (a) Using DF flag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions.
   (b) Discuss the importance of procedures in assembly language programming? [10+6]
6. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?

(b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? [8+8]

7. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7?

   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]

8. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?

   (a) PCON

   (b) PSW

   (c) IP

   (d) TMOD [4x4=16]

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Code No: RR322203 **RR** **Set No. 3**

III B.Tech II Semester Examinations,December 2010
MICROPROCESSORS AND MICRO CONTROLLERS
Instrumentation And Control Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?
   (b) Explain single transfer mode and block transfer mode of 8237? [8+8]
2. (a) Discuss the organization of FLASH memory? Explain FLASH memory command definitions?
   (b) Why do you need wait states? Explain how wait states are generated?
   (c) Give possible solutions to meet the processor access time requirements when memory is interfaced to the processor? [7+4+5]
3. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? [8+8]
4. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
   (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
   (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
   (c) Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
   (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]
5. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
   (a) PCON
   (b) PSW
   (c) IP
   (d) TMOD [4x4=16]

6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7?

   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]

7. (a) Using DF flag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions.

   (b) Discuss the importance of procedures in assembly language programming? [10+6]

8. (a) Discuss the system bus cycle of 8086 with a neat diagram? What is the use of wait cycles? Compare wait and idle cycles?

   (b) Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086? [8+8]

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