Code No: **PT41043** **R13** **Set No. 1**

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017

ANALOG IC DESIGN

(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) Define threshold voltage and derive an expression for it. [4]
   b) Explain about current sink and current sources. [4]
   c) Explain the working of a class A output amplifier. [4]
   d) Explain the slew rate for p-channel differential amplifier with necessary equations [4]
   e) Discuss the dynamic characteristics of a Comparator [3]
   f) What is a ring oscillator and explain its operation. [3]

PART–B *(3x16 = 48 Marks)*

2. a) Explain the fabrication of resistors and capacitors in integrated circuit technology [8]
   b) Draw and explain the various components of large signal model of a MOS Transistor. [8]

3. a) Derive the expression for the sensitivity of a pn junction voltage reference circuit using MOSFET. [8]
   b) Discuss about Band gap references. [8]

4. a) Perform the analysis of CMOS differential amplifiers. [8]
   b) Explain the various architectures of high gain amplifiers. [8]

5. a) Explain any one of the concept of compensation of two stage CMOS Op-Amp. [8]
   b) Discuss about the cascade op-amp. [8]

6. a) Explain about Switched Capacitor Comparators. [8]
   b) Explain the auto zeroing concept of improving the performance of a comparator. [8]

7. a) Derive the expression for the frequency of oscillation of an LC oscillator. [8]
   b) Explain how a PLL can be used in frequency multiplication and synthesis. [8]