Code No: **RT41044** **R13** **Set No. 1**

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017

COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1. a) Describe about memory unit. [4]
   b) Discuss various types of Interrupts. [4]
   c) Define Microinstruction. [3]
   d) What do you mean by content addressable memory? [4]
   e) What is the difference between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each? [5]
   f) What do you mean by delayed load? [2]

PART–B *(3x16 = 48 Marks)*

2. a) Distinguish between fixed point representation and floating point representation. [8]
   b) Represent the number $(+46.5)_{10}$ as a floating-point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits. [8]

3. a) What are the basic differences among a branch instruction, a call subroutine instruction, and program interrupt? [8]
   b) Construct a bidirectional shift register with parallel load and give the function table of the circuit. [8]

4. a) Give an overview of address sequencing in microprogrammed control unit. [8]
   b) Formulate a mapping procedure that provides eight consecutive microinstructions for each routing. The operation code has six bits and the control memory has 2048 words. [8]

5. a) Explain the functionalities of memory management hardware. [8]
   b) Explain various mapping procedures of cache memory with an example. [8]

6. a) Demonstrate how communication proceeds between CPU and IOP. [8]
   b) Explain in detail various I/O modes of transfer. [8]

7. a) Illustrate arithmetic pipeline with an example. [8]
   b) Derive speedup achieved by a pipeline unit over a non-pipeline unit. [8]

Code No: **RT41044** **R13** **Set No. 2**

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COMPUTER ARCHITECTURE AND ORGANIZATION

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1. a) Describe about Arithmetic Logic Unit. [4]
   b) Describe the basic Instruction format. [4]
   c) Define Micro-operation. [4]
   d) What is the purpose of cache memory? [3]
   e) Define cycle stealing. [3]
   f) Write about Pipeline conflicts. [4]

PART–B *(3x16 = 48 Marks)*

2. a) Demonstrate the procedure for obtaining product-of-sums using k-maps. [8]
   b) Define $(r-1)$'s complement and r's complement. [8]

3. a) Give the major characteristics of RISC and CISC architectures. [8]
   b) What are addressing modes? Give an overview of the addressing modes. [8]

4. a) Distinguish between microprogrammed and hardwired control unit. [8]
   b) What are the microinstructions needed for the fetch routine? Explain. [8]

5. a) A computer employs RAM chips of 256×8 and ROM chips of size 1024×8. Extend the memory system to 4096 bytes of RAM and 4096 bytes of RAM. List the memory address map and indicate what size decoders are needed. [8]
   b) Demonstrate with an example address mapping using pages. [8]

6. a) Design parallel priority interrupt hardware for a system with eight interrupt sources. [8]
   b) What is direct memory transfer? Give an overview and the block diagram of a DMA controller. [8]

7. a) Illustrate with an example hardware implementation of division algorithm. [8]
   b) What are the pipeline conflicts that cause the instruction pipeline to deviate from its normal operation? [8]

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Code No: **RT41044** **R13** **Set No. 3**

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017

COMPUTER ARCHITECTURE AND ORGANIZATION

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1.	a)	Describe about control unit.	[4]
	b)	Describe the phases of instruction cycle briefly.	[5]
	c)	Define microprogram.	[3]
	d)	What do you mean by bootstrap loader?	[4]
	e)	What do you mean by vectored interrupt?	[3]
	f)	Write about delayed branch.	[3]

PART–B *(3x16 = 48 Marks)*

2.	a)	Describe fixed point representation and floating point representation.	[8]
	b)	Give an overview of the basic functional units and bus structures of a computer.	[8]
3.	a)	An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow	[8]
	b)	Give few examples of external interrupts and few examples of internal interrupts. What is the difference between a software interrupt and subroutine call.	[8]
4.	a)	What are main types of control units? Explain briefly.	[8]
	b)	Give the block diagram of a control memory and the associated hardware needed for selecting the next micro-instruction address.	[8]
5.	a)	Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 µs; level 2 contains 1,00,000 words and has an access time of 0.1µs. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose, we ignore the time required to determine whether the word is in level 1 or level 2 and 95% of the memory accesses are found in the cache, then what is the average access time of a word.	[8]
	b)	What is cache memory? What are its advantages? Explain.	[8]
6.	a)	Demonstrate interrupt-initiated I/O.	[8]
	b)	Explain the functionalities of an IOP interface unit.	[8]
7.	a)	Illustrate with an example an instruction pipeline.	[8]
	b)	Illustrate with an example Booth multiplication algorithm.	[8]

Code No: **RT41044** **R13** **Set No. 4**

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017

COMPUTER ARCHITECTURE AND ORGANIZATION

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1. a) Distinguish among computer organization and computer architecture. [4]
   b) What do you mean by register transfer language? What are the uses of register transfer language? [4]
   c) Define Microcode. [3]
   d) What do you mean by associative memory? Give applications of associative memory. [5]
   e) What do you mean by multiprogramming? [3]
   f) Describe about MIMD. [3]

PART–B *(3x16 = 48 Marks)*

2. a) Illustrate with examples fixed point representation and floating point representation. [8]
   b) Give an overview of the performance measurement of computers. [8]

3. a) Using a 4-bit counter with parallel load and a 4-bit adder, draw a block diagram that shows how to implement the following statements:

   x: R1←R1+R2 Add R2 to R1

   x'y: R1←R1+1 Increment R1

   where R1 is a counter with parallel load and R2 is a 4-bit register [8]
   b) Explain the functionalities and applications of the following:
      i. Decoders ii. Encoders
      iii. Multiplexers iv. De-multiplexers [8]

4. a) What is the difference between a microprocessor and microprogram? Is it possible to design a microprocessor? [8]
   b) Explain how address sequencing is done in a microprogrammed control unit. [8]

5. a) Demonstrate logical to physical address mapping using segmented-paging. [8]
   b) What is virtual memory? Explain. [8]

6. a) Give an overview of parallel priority interrupt hardware. [8]
   b) Demonstrate the mechanism of DMA. [8]

7. a) Illustrate with an example an arithmetic pipeline. [8]
   b) Give the flowchart of addition and subtraction of two floating-point binary numbers. [8]