Code No: **R31041** **R10** **Set No. 1**

III B.Tech I Semester Supplementary Examinations, May - 2017

COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Electronics and Communications Engineering**,** Electronics and Instrumentation Engineering**)**

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1	a)	Explain about the Bus interconnections.	[7M]
	b)	Explain integer representation with an example.	[8M]
2	a)	List and explain the characteristics of machine instructions.	[8M]
	b)	Discuss instruction pipelining in detail.	[7M]
3	a)	Explain in detail about micro instruction execution.	[8M]
	b)	Hardwired control unit is faster than micro programmed control unit. Justify this statement.	[7M]
4	a)	Explain the Booth's algorithm for multiplication of signed two's complement numbers.	[8M]
	b)	Discuss hardware algorithm for addition & subtraction using flowchart.	[7M]
5	a)	Explain briefly about memory management hardware.	[8M]
	b)	Write short notes on set-associative mapping.	[7M]
6	a)	Write short notes on the following: **i**. Serial communication **ii**. DMA.	[8M]
	b)	Discuss about asynchronous data transfer.	[7M]
7	a)	Illustrate vector computations with example.	[8M]
	b)	Explain in detail about non-uniform memory access computers.	[7M]
8	a)	Explain various mechanisms for achieving synchronization in multiprocessor systems.	[8M]
	b)	Write short note on multiport memory.	[7M]

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