Code No: **PT41048** **R13** **Set No. 1**

**IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017**

# DIGITAL IC DESIGN

**(Electronics and Communication Engineering)**

**Time: 3 hours** **Max. Marks: 70**

***Question paper consists of Part-A and Part-B***
***Answer ALL sub questions from Part-A***
***Answer any THREE questions from Part-B***
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## PART–A *(22 Marks)*

| | | | |
|---|---|---|---|
| 1. | a) | Compare CMOS technology with Bipolar technology. | [4] |
| | b) | What is the Latch-up in CMOS circuits? Explain it. | [4] |
| | c) | Design SR Latch and explain its function. | [3] |
| | d) | Explain Pass transistor circuits. | [4] |
| | e) | What is the need of interconnect? | [3] |
| | f) | Distinguish between SRAM and DRAM. | [4] |

## PART–B *(3x16 = 48 Marks)*

| | | | |
|---|---|---|---|
| 2. | a) | What are the criteria for voltage threshold for high level and low level in NMOS inverter characteristics? Explain. | [8] |
| | b) | Determine pull-up to pull-down ratio for an NMOS inverter driven through one or more pass transistors. | [8] |
| 3. | a) | How the MOS inverters connected in cascade can drive large capacitive loads? Explain. | [8] |
| | b) | Draw the CMOS full adder circuit and explain its operation. | [8] |
| 4. | a) | Explain about CMOS D Latch and Edge triggered flip-flop. | [8] |
| | b) | Explain the behavior of bistable elements. | [8] |
| 5. | a) | With an example, briefly explain about the principle of voltage bootstrapping. | [8] |
| | b) | Design and explain the high performance dynamic CMOS circuits. | [8] |
| 6. | a) | Explain in detail with help of capacitive parasitics interconnect. | [8] |
| | b) | Discuss the advanced interconnect techniques. | [8] |
| 7. | a) | What are the types of DRAM? Explain any one. | [8] |
| | b) | Explain the NOR flash and NAND flash memory techniques. | [8] |