Code No: **R31042 R10**

Set No. 1

III B.Tech I Semester Supplementary Examinations, May-2017 DIGITAL IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Bio Medical Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 75 **Answer any FIVE Questions** All Questions carry equal marks **** 1 a) Draw the circuit diagram, functional table and logic symbol of CMOS OR gate [8] and explain its operation b) Explain the terms Fan- in and Fan- out of a CMOS Inverter along with circuit [7] diagram 2 a) Draw the circuit diagram of two-input 10 K ECL NOR gate and explain the [7] operation of it b) Explain the following terms with reference to TTL gate [8] (ii)D.C noise margin (iii)Low-state unit load (i)Logic levels (iv) High-state fan-out 3 a) Design a 16x1 multiplexer using two 74x151 multiplexer and one 74x139 [8] decoder b) Draw the logic circuit for binary to BCD Code convertor and explain its [7] operation 4 a) Draw the block diagram of Binary Adder and Subtractor and explain its [10] operation in detail b) Write short notes on Dual Priority Encoder in detail [5] 5 a) Draw the edge trigger D flip flop and explain its operation along with timing [8] diagram b) Design a 4-bit binary synchronous counter using 74x74 and explain its [7] operation in detail 6 a) Design an 8-bit parallel-in and serial-out shift register and Explain the [8] operation with the help of timing diagram b) Write short notes on MSI Shift Registers in detail with one example [7] 7 Implement the following Boolean functions using PAL, PLA and PROM [15] $f1(A,B,C,d) = \sum m(0,1,2,4,6,8,10,12,15)$ $f2(A,B,C,d) = \sum m(0,2,6,7,8,11,13,15)$ 8 a) Draw the internal circuit diagram of 4T Static RAM and explain its operation. [8] b) List out few comparisons of SRAM verses DRAM along with advantages and [7]

disadvantages.
