

Code No: RT31044

R13

SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2017

DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

(Common to Electronics and Communications Engineering, Electronics and Instrumentation Engineering)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)

2. Answering the question in **Part-A** is compulsory

3. Answer any **THREE** Questions from **Part-B**

PART -A

- 1 a) Discuss the behavioral model of a flip flop. [3M]
- b) What is a technology library? Discuss. [4M]
- c) Compare ROM, PLA and PAL. [4M]
- d) Give the characteristics of TTL logic family. [3M]
- e) What is a floating point encoder? explain [4M]
- f) Discuss the modes of operation of shift registers. [4M]

PART –B

- | | | |
|---|--|-------|
| 2 | a) What is the difference between the sequential from concurrent signal assignment statements? | [4M] |
| | b) Discuss the sequential assignment statements with examples. | [8M] |
| | c) Brief the objects in VHDL. | [4M] |
| 3 | a) What are the operations performed by a logic simulator. | [8M] |
| | b) Why place and route tools are used in VHDL draw the data flow diagram of place and route tools and explain. | [8M] |
| 4 | a) Design an 8x4 diode ROM using 74x138 for the following data from the first location 1,4,9, B,A,O,F,C | [8M] |
| | b) Draw the read and write cycle timing diagrams and explain the read and write operation of SSRAM. | [8M] |
| 5 | a) Draw a two input 10K ECL OR gate and verify the truth table. | [8M] |
| | b) Explain the circuit behavior of CMOS with non ideal outputs. And compare the CMOS logic families. | [8M] |
| 6 | Design a 8bit ALU using two 74LS181 ICs. | [16M] |
| 7 | a) Design a 3 bit LFSR with an initial state of 6. | [8M] |
| | b) Design a modulo 11 counter using 74x163. | [8M] |
