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Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2017

DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

(Common to Electronics and Computer Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Write the features VHDL.	[3M]
	b)	Write a test bench for two input NAND gate using VHDL.	[4M]
	c)	Compare PLA and PAL.	[3M]
	d)	What are the advantages of ECL gates?	[4M]
	e)	Write a VHDL program for8X3 encoder.	[4M]
	f)	Write VHDL code for T Flip Flop with asynchronous reset using behavioural modelling.	[4M]

PART -B

2	a)	Explain in detail about Elements in VHDL.	[8M]
	b)	Discuss libraries and packages n detail	[8M]
3	a)	What is the importance of static Timing in VHDL and explain its function?	[8M]
	b)	Discuss some of the important factors related to Simulation.	[8M]
4	a)	Implement 4X1 multiplexer using ROM.	[12M]
	b)	Classify PLDs and memories.	[4M]
5	a)	Explain the CMOS circuit behavior with resistive load.	[8M]
	b)	Explain about CMOS/TTL interfacing.	[8M]
6	a)	Design and discuss barrel shift.	[8M]
	b)	Write VHDL code for Barrel Shifter.	[8M]
7		Design, explain and write VHDL code for Universal Shift Register.	[16M]

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DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

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Time: 3 hours Max. Marks: 70

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the comparison of VHDL and Verilog HDL.	[3M]
	b)	Explain about Functional simulation.	[4M]
	c)	Compare ROM and PLA.	[4M]
	d)	Describe the key benefit of schottky transistors in TTL.	[3M]
	e)	Write VHDL code for half subtractor using structural modeling.	[4M]
	f)	Write the difference between latches and flip flops.	[4M]

PART -B

2	a)	Explain about dataflow design elements of VHDL.	[8M]
	b)	Write VHDL Code of 8 x 1Mux using data flow.	[8M]
3	a)	Explain about the logic synthesizer.	[8M]
	b)	Explain in detail about Post Layout Timing Simulation.	[8M]
4	a)	Describe in detail about DRAM with an appropriate diagram and explain about its timings.	[8M]
	b)	Draw a logic symbol for and determine the size of a ROM that realizes an 8X8 combinational multiplier.	[8M]
5	a)	Explain the CMOS circuit behavior with non ideal inputs.	[8M]
	b)	Design a 4 input CMOS AND-OR-INVERT gate. Explain the circuit with the help of logic diagram and function table.	[8M]
6	a)	Implement the 32 input to 5 output priority encoder using four 74LS148 gates.	[8M]
	b)	Design a 4×4 combinational multiplier and write the VHDL program in data flow model.	[8M]
7	a)	Design a 8 bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.	[8M]
	b)	Write a VHDL code for Ring counter.	[8M]

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Explain about Data Objects.	[4M]
	b)	Define logic synthesis.	[3M]
	c)	Write the applications of SRAM.	[3M]
	d)	What are features of TTL logic family?	[4M]
	e)	Write VHDL program for 4X1 multiplex.	[4M]
	f)	Write Modes of Operation of Shift Registers.	[4M]

PART -B

2	a)	Explain about Levels of Abstraction.	[8M]
	b)	Write a VHDL code for aaa4 bit counter using behavioral modeling.	[8M]
3	a)	What is the importance of time dimension in VHDL and explain its function.	[8M]
	b)	Explain with data flow diagram about why place and route tools are used in VHDL.	[8M]
4	a)	Explain the block diagram operation of Synchronous RAM.	[8M]
	b)	Implement Full adder using PAL.	[8M]
5	a)	Explain dynamic electrical behavior of a CMOS.	[8M]
	b)	Draw and explain the 2-input OR/NOR gate using ECL logic.	[8M]
6		Design and Discuss carry look ahead carry generator.	[16M]
7	a)	Explain in detail about the working of Johnson Counter using 74 LS194.	[8M]
	b)	Discuss the logic circuit of 74×377 register. Write a VHDL program for the same in structural style.	[8M]

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Write the syntax for Package.	[3M]
	b)	Discuss about Technology Libraries.	[4M]
	c)	Distinguish between SRAM and DRAM.	[4M]
	d)	What are the disadvantages of ECL gates?	[3M]
	e)	Mention all types of tri state buffers.	[4M]
	f)	Write a VHDL code for a 4 bit down counter.	[4M]

PART -B

2	a)	Write a VHDL code for a full adder using two half adders in structural modeling.	[12M]
	b)	Write short notes on sub programs.	[4M]
3		Write short notes on (a) technology libraries. (b)Place and route (c) Netlist formats	[16M]
4	a)	Explain with timing diagrams of read and write operation of SSRAM.	[8M]
	b)	Implement the following Boolean functions using a PLA $F_1(A,B,C) = \Sigma m(1,2,3,7)$; $F_2=(A,B,C) = \Sigma m(0,1,5)$.	[8M]
5	a)	Discuss the behaviour of a CMOS as an inverter. i) Inductive effects ii) Propagation delay	[8M]
	b)	Draw the circuit diagram of basic TTL NAND gate and explain with the help of functional operation.	[8M]
6	a	Write the VHDL code for 16 bit barrel shifter .	[8M]
	b	Design a 4bit carry look ahead adder using gates and write the VHDL code for it.	[8M]
7	a)	Write a VHDL program to design a modulo-8 counter.	[8M]
	b)	Write a VHDL program to simulate the behaviour of a positive edge triggered J-K flip – flop.	[8M]

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