Code No: R1621053 **R16** SET - 1

II B. Tech I Semester Model Question Paper Oct/Nov - 2017
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A [7 x 2 =14]

1. a) Convert the following numbers with the given radix to decimal.
i) $(4433)_5$ ii) $(1199)_{12}$
b) State and prove De Morgan's theorem.

Define encoder? List out the applications of it?

c) Explain the operation of a SR flip-flop?
d) Discuss about a serial-in, serial-out shift registers?
e) Compare a decoder with a Demultiplexer.
f) What are the basic operations in Boolean algebra?

PART –B

2. a) Perform the subtraction using 1's complement and 2's complement methods. (7M)
i) 11010 – 10000 ii) 11010 – 1101 iii) 100 - 110000
b) How are negative numbers represented? Represent signed numbers from +7 to -8 using different ways of representation. (7M)

3. a) Reduce using mapping the following expression and implement the real minimal expression in Universal logic. F= ∑m (0, 2, 4, 6, 7, 8, 10, 12, 13, 15) (7M)
b) State and prove consensus theorem? Solve the given expression using consensus theorem. (i) $\overline{AB} + AC + \overline{BC} + \overline{BC} + AB$ (ii) $(A + B)(A + C)(B + C)(A + D)(B + D)$ (7M)

4. a) Perform the realization of half adder and full adder using decoders and logic gates. (7M)
b) Design a 4 bit combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR Gates. (7M)

5. a) Draw the circuit diagram of a positive edge triggered JK flip flop and explain its operation with the help of a truth table? (7M)
b) Convert a D flip flop into SR flip flop and JK flip flop? (7M)

6. a) Design a 4-bit universal shift register using D flip flops and multiplexers? (7M)
b) Explain the operation of 4-bit ring counter with circuit diagram, state transition diagram and state table. Draw the corresponding timing diagrams? (7M)

7. a) Express the complement of the following functions in sum-of-minterms form:
i)F(A,B ,C, D) = ∑(2, 4, 7, 10, 12, 14) ii) F (x, y, z) = π(3, 5, 7). (7M)
b) List out the basic theorems and properties of Boolean Algebra. (7M)

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

[7 x 2 =14]

1. a) Why is hexadecimal code widely used in digital systems? List out the digits used to represent the hexadecimal codes?
   b) What is two-level logic? What is its advantage?
   c) Why a multiplexer is called a data selector? Draw the 2x1 MUX.
   d) What are the various methods used for triggering flip-flops? Explain with examplesexamples.
   e) Explain the basic types of shift registers?
   f) State the purpose of reducing the switching functions to minimal form.
   g) What are the characteristics of 2's complement numbers?

PART –B

2. a) Subtract the following decimal numbers by the 9's and 10's complement methods. (7M)
   274 - 86 ii) 93 - 615 iii) 574.6 - 297.7 iv) 376.3 -765.6
   b) What is a Gray code? Obtain a 3-bit and 4-bit gray code from a 2-bit gray code by reflection. (7M)

3. a) Without reducing, implement the following expressions in AOI logic and then convert them into NAND logic and NOR logic (7M)
   A + BC + (A + B'C) + D ii) A + B'C + (B + C)' + B'C'
   b) Reduce the following expression to the simplest possible POS and SOP forms. (7M)
   $F = \sum m(6,8,13,18,19,25,27,29,31) + d(2,3,11,15,17,24,28)$

4. a) Implement the following multiple output combinational logic circuit using a 4 line to 16 line decoder: (7M)
   $F_1 = \sum m(0, 1, 4, 7, 12, 14, 15)$ $F_3 = \sum m(2, 3, 7, 8, 10)$
   $F_2 = \sum m(1, 3, 6, 9, 12)$ $F_4 = \sum m(1, 3, 5)$
   b) Discuss a few applications of multiplexers and distinguish between a multiplexer and a decoder. (7M)

5. a) Draw the schematic circuit of an edge-triggered JK flip flop with active low preset and active low clear using NAND gates and explain its operation? (7M)
   b) Define the following terms with relation to flip flop: (7M)
   i) Set-up time ii) Hold time iii) Propagation delay time iv) Preset v) Clear

6. a) Design a type-D counter that goes through states 0, 2, 4, 6, 0…….. The undesired states must always go to a 0 on the next clock pulse. (7M)
   b) With suitable logic diagram explain a 4-bit bidirectional shift register? (7M)

7. a) Find the complement of F = wx + yz; then show that FF' = 0 and F + F' = 1. (7M)
   b) List the truth table of the function: i) F = xy + xy' + y'z ii) F = bc + a'c' (7M)

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

[7 x 2 =14]

1. a) What are the three methods of obtaining the 2's complement of a given binary number?
   b) How can a NOR gate be used as an inverter, AND gate and OR gate?
   c) Distinguish between a half-adder and a full-adder?
   d) Draw the circuit of J – K master slave flip-flop with active high clear and active low preset.
   e) Draw the state diagram of modulo-4 up/down counter.
   f) How are negative numbers represented?
   g) Define full Subtractor.

PART -B

2. a) How are binary codes classified? Briefly explain each code with suitable examples? (7M)
   b) Convert the following numbers into Gray code numbers (7M)
   i) $(96)_{10}$ ii) $(45)_{16}$ iii) $(235)_{8}$ iv) $(85)_{12}$

3. a) Simplify the following using K- map and implement the same using NAND gates. (7M)
   $Y(A, B, C) = \sum (0, 2, 4, 5, 6, 7)$
   b) Simplify the following Boolean expression. (7M)
   T(x, y, z) = (x + y) {[x' (y' + z')]'} +x' y' +x' z'
   $X(A, B, C, D) = A^1B^1C^1+(A+B+C^1)^1+A^1B^1C^1D$

4. a) Draw the logic diagram of a 2 to 4 line decoder using NOR gates including an enable input. (7M)
   b) Give circuit implementation of 4 Bit Ripple adder and Ripple Adder/Subtractor using ones and twos complement method. (7M)

5. a) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation? (7M)
   b) Give the transition table for SR, JK, D and T flip flops. Convert an SR flip flop into D flip flop. (7M)

6. a) Write the design steps of synchronous counters with suitable examples? (7M)
   b) What is a register? Discuss the applications of shift registers? (7M)

7. a) Express the following function as a sum of minterms and as a product of maxterms: (7M)
   F(A, B, C, D) = B'D + A'D + BD

   b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa. (7M)

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

[7 x 2 =14]

1. a) How are negative numbers represented?
   b) What do you mean by K-map? Name it advantages and disadvantages.
   c) What is meant by race around condition in flip-flops?
   d) Draw and explain active low S-R latch.
   e) Draw the state diagram of synchronous mod-10 up-down counter.
   f) Write the Boolean algebraic laws.
   g) What is a standard SOP form?

PART -B

2. a) Convert the following to Decimal and then to octal (7M)
   (i) $(125F)_{16}$ (ii) $(10111111)_2$ (iii) $(392)_{10}$
   b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property? (7M)

3. a) Simplify the following using K- map and implement the same using NAND gates. (7M)
   Y (A, B, C) = ∑ (0, 2, 4, 5, 6, 7)
   b) Represent and draw the following Boolean function using minimum number of basic gates. i) (AB + AB') (AB)' (7M)
   ii) [(ABD(C + D + E)) + (A +DBC)'] (ABC + (CAD)')

4. a) Realize the function f(A,B,C,D) = ∑ (1,2,5,8,10,14)+d (6,7,15) using (7M)
   i) 8:1 MUX ii) 4:1 MUX
   b) Design and draw the logic circuit diagram for full adder/subtractor. Let us consider a control variable w and the designed circuit that functions as a full adder when w=0, as a full subtractor when w= 1. (7M)

5. a) Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation. Explain the Race around condition and also explain how to eliminate it. (7M)
   b) Draw the circuit diagram of clocked D-flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram. (7M)

6. a) Explain the operation of 5-stage twisted ring counter with circuit diagram, state transition diagram and state table. (7M)
   b) With suitable logic diagrams explain about Buffer register and Controlled buffer register? (7M)

7. a) Determine whether the following Boolean equation is true or false. x'y' + x'z + x'z' = x'z' + y'z' + x'z (7M)
   b) Show that the dual of the exclusive-OR is equal to its complement. (7M)
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