Code No: R1621053 **R16** SET - 1

II B. Tech I Semester Regular Examinations, October/November - 2017
DIGITAL LOGIC DESIGN
(Com to CSE & IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Find the 10's complement of 3826.
b) Find the complement of the function: $A'B(C+D)+B'C'+AB'C$.
c) Draw the 4-varaiable K-map.
d) Write the truth table of a full subtractor.
e) What is a state diagram?
f) Write the differences between the Combinational and sequential circuits.

PART -B

2. a) Convert the following numbers to Octal:
(i) $(1011.1010)_2$
(ii) $(BABA)_{16}$
b) Perform the binary subtraction using 1's and 2's complement methods.
$(110011)_2$-$(1110011)_2$

3. a) Convert the given Boolean function into standard sum of minterms form.
$F = x'y+y'z+xz$
b) Explain the theorems and properties of Boolean algebra.

4. Simplify the following Boolean function
F(A, B, C, D)= Σ(0, 6, 8, 13, 14); d(A, B, C, D)=Σ(2, 4,10)
using K-Map method in (a)SOP form (b) POS form

5. a) Design a full subtractor circuit with basic gates.
b) Write the HDL dataflow description of a 8X1 multiplexer.

6. a) Explain the operation of a JK flip-flop with the truth table.
b) Draw the diagram of Mealy type state machine for serial adder and explain its operation.

7. a) Design a decade counter using T flip-flops.
b) Explain the operation of a 4-bit shift register using RS flip-flops.
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Code No: R1621053 **R16** SET - 2

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) What are the universal gates? Why they are called as universal gates?
   b) What is Minterm and Maxterm
   c) Define the essential prime implicants in a K-map method.
   d) What is a multiplexer? Write its applications.
   e) What is a mealy machine
   f) Write the differences between the synchronous and asynchronous sequential circuits.

PART -B

2. a) Convert the following numbers to Binary:
   (i) $(59.425)_{10}$
   (ii) $(46BF)_{16}$
   b) Perform the subtraction in binary using 1's and 2's complement methods.
   $(255)_{10} - (408)_{10}$

3. a) Convert the following Boolean function into standard product of maxterms form.
   $$F = A'B+C+B'D'$$
   b) State and prove the De Morgan's laws.

4. Simplify the following Boolean function
   F(A, B, C, D)= Σ(1,3,8,10,15); d(A, B, C, D)=Σ(0, 2, 9)
   using K-Map method in
   (a) SOP form (b) POS form

5. a) Design an 8X1 multiplexer with basic gates.
   b) Write the gate level HDL description of the 4:16 decoder.

6. a) What is the drawback of JK flip-flop? How is it eliminated in Master Slave flip-flop? Explain with diagram
   b) What are the capabilities and limitations of finite state machines? Explain.

7. a) Design a modulo-10 ripple counter using RS flip-flops.
   b) Explain the operation of a 4-bit shift register using T flip-flops.
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R16

SET - 3

II B. Tech I Semester Regular Examinations, October/November - 2017
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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Find the 1's and 2's complement of the decimal number 101.
   b) What is a canonical form
   c) What do you mean by don't care combinations.
   d) What is a de-multiplexer? Write its applications.
   e) Write the features of Moore machine.
   f) What are the differences between Johnson and ripple counter.

PART -B

2. a) Convert the following number to Hexadecimal:
   (i) $(925.25)_8$
   (ii) $(1111010.10)_2$
   b) Perform the binary subtraction using 1's and 2's complement method.
   $(1111101)_2 - (100111110)_2$

3. a) Write the theorems and postulates of Boolean algebra.
   b) Reduce the following Boolean function to four literals and draw the logic diagram: $(A'+C)(A'+C')(A+B+C'D)$

4. Simplify the following Boolean function
   $F(A, B, C, D)=\Sigma(2, 4, 6, 10, 12); d(A, B, C, D)=\Sigma(0, 8, 9, 13)$
   using K-Map method in
   (a) SOP form (b)POS form

5. a) Design a 4-bit binary adder-subtractor circuit with basic gates.
   b) Write an HDL dataflow description of a 4-bit adder-subtractor circuit of unsigned numbers.

6. a) Explain the operation of JK master-slave flip-flop.
   b) Obtain the state table and state diagram for a sequence detector to recognize the occurrence of sequence bits 110 & 001.

7. a) Design a Mod-10 counter using RS flip-flops
   b) Explain the operation of a 4-bit shift register using JK flip-flops.
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Code No: R1621053 **R16** SET - 4

II B. Tech I Semester Regular Examinations, October/November - 2017
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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Convert the binary number 10111001 to gray code.
   b) Write the basic Boolean theorems.
   c) Draw the 5-variable K-Map.
   d) What is a decoder? Write its applications.
   e) What is a Flip flop
   f) What is a Ring counter.

PART -B

2. a) Express the following numbers in decimal:
   (i) $(126.25)_8$
   (ii) $(166.425)_{16}$
   b) Perform the subtraction in binary using 1's and 2's complement methods.
   $(97)_{10} - (255)_{10}$

3. a) Find the dual and complement of the following function:
   $A'BD'+B'(AC'+D')+A'BC'$
   b) Implement the following Boolean function with only two input NOR gates:
   $F=(AB'+D')E+C(A'+B'D)$

4. a) Simplify the following Boolean function with the don't conditions *d* using K-map method:
   F(A, B, C, D)=Σ(4, 5, 7, 12, 13, 14); d(A, B, C, D)=Σ(1, 9, 11, 15)
   b) Realize the simplified expression obtained in Q. 4(a) with only NAND gates.

5. a) Design a 4:16 decoder with basic gates.
   b) Write an HDL behavioral description of a 16X1 multiplexer.
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Code No: R1621053 **R16** SET - 4

6. a) Explain the D flip-flop with the help of truth table and excitation table.

   b) Convert the following Mealy machine into a corresponding Moore machine.

PS	NS, Z	
	X=0	X=1
A	C, 0	B, 0
B	A, 1	D, 0
C	B, 1	A, 1
D	D, 1	C, 0

7. a) Design a Mod-12 counter using D flip-flops.

   b) Explain the operation of a 4-bit shift register using D flip-flops.