

Code No: RT21053

R13

SET - 1

II B. Tech I Semester Supplementary Examinations, May/June - 2017

DIGITAL LOGIC DESIGN

(Com. to CSE, IT)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)

2. Answer **ALL** the question in **Part-A**

3. Answer any **THREE** Questions from **Part-B**

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**PART -A**

1. a) Write first 20 numbers in radix-5 (3M)
- b) Convert the following to the other canonical form:  $F(x, y, z) = \sum(1, 3, 5)$  (4M)
- c) Implement function  $f = AB + \bar{A}B$  using 2X1 MUX (4M)
- d) What is sequential circuit? (3M)
- e) Write the between register and counter (4M)
- f) Draw the block diagram of PLA (4M)

**PART -B**

2. a) Obtain the 1's and 2's complement of the following binary numbers 1010101 , 0111000 , 0000001 , 10000 , 00000 Also obtain 9's and 10's complement of the following decimal numbers 09900 , 10000 , 00000 (8M)
- b) What is a reflected code? Write about reflected codes by giving examples. (8M)
3. a) Show that the dual of the exclusive-OR is equal to its complement (8M)
- b) Draw a NAND logic diagram that implements the complement of the following function:  $F(A, B, C, D) = \sum(0, 1, 2, 3, 6, 10, 11, 14)$  (8M)
4. a) Implement a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to- 4-line decoder (8M)
- b) Design 4 bit Magnitude Comparator and explain in detail (8M)
5. a) What is difference between latch and flip flop? Explain about clocked RS flip flop using NAND gates (8M)
- b) Conversion of SR Flip Flop to JK Flip Flop (8M)
6. a) Design a shift register with parallel load operations according to the following function table: (8M)

| shift | load | Register operation |
|-------|------|--------------------|
| 0     | 0    | No change          |
| 0     | 1    | Load parallel data |
| 1     | X    | Shift right        |

- b) Construct and explain a Johnson counter for ten timing signals (8M)
  7. a) Write the difference between PROM, PLA and PAL (8M)
  - b) A Combinational circuit defined by functions (8M)
- $$F_1(A, B, C) = \sum(3, 5, 6, 7) \quad F_2(A, B, C) = \sum(0, 2, 4, 7)$$
- Implement circuit with PLA