

Code No: R1621041

R16**SET - 1****II B. Tech I Semester Regular Examinations, October/November - 2017****ELECTRONIC DEVICES AND CIRCUITS**

(Com to ECE, EIE and ECC)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)2. Answer **ALL** the question in **Part-A**3. Answer any **FOUR** Questions from **Part-B**

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**PART -A**

1. a) What is intrinsic semiconductor? (2M)
- b) Write the disadvantages of LED (2M)
- c) Define Ripple factor and peak inverse voltage (3M)
- d) Write the applications of JFET (2M)
- e) What are the advantages of self-biasing circuit? (3M)
- f) What is emitter follower? (2M)

**PART -B**

2. a) Explain in detail about Hall effect (7M)
- b) Calculate the resistivity of intrinsic germanium at  $300^{\circ}K$ . Assume  $n_i = 2 \times 10^{13} \text{ per cm}^3$ ,  $\mu_n = 3800 \text{ cm}^2/\text{V-s}$  and  $\mu_p = 1800 \text{ cm}^2/\text{V-s}$  (7M)
3. a) Explain the formation of depletion region in a PN junction (7M)
- b) A P-N junction silicon diode has a reverse saturation current of 50nA at room temperature  $27^{\circ}K$ . If the new reverse saturation current is observed to be 160nA, calculate the value of new temperature. (7M)
4. a) Draw and explain the circuit diagram of full wave rectifier with L-section filter (7M)
- b) In half-wave rectifier an ac voltage of peak value 24V is connected in series with silicon diode and load resistance of  $480\Omega$ . If the forward resistance of the diode is  $20\Omega$ , find average load current and rms value of load current. (7M)
5. a) Explain input and output characteristics of a transistor in CB configuration (7M)
- b) A certain JFET operates in the linear region with a constant drain voltage of 1V. When the gate voltage is 2V, a drain current of 10mA flows, but when gate voltage is changed to 1V, the drain current becomes 22.8mA. Find (a) the pinch-off voltage (b) the channel resistance for zero gate voltage (7M)
6. a) Explain any two bias compensation techniques (7M)
- b) An npn transistor if  $\beta=50$  is used in CE circuit with  $V_{CC} = 10V$ ,  $R_C = 2k\Omega$ . The bias is obtained by connecting  $100k\Omega$  resistor from collector to base. Find the quiescent point and stability factor. (7M)

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**SET - 1**

7. a) Draw the h-parameters equivalent circuit for a common emitter amplifier and (7M)  
derive the Expression for  $A_i$ ,  $R_i$ ,  $A_v$ .
- b) Compare the performance of BJT as an amplifier in CE, CB, CC configuration (7M)

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**SET - 2**

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2. Answer **ALL** the question in **Part-A**

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PART -A

1. a) What is meant by doping in semiconductor? (2M)
- b) Write the advantages of photo diode (2M)
- c) Define Transformer utilization factor (2M)
- d) Why are n-channel MOSFETs preferred over P-channel MOSFET? (3M)
- e) What are the advantages of fixed biasing circuit? (2M)
- f) What is an amplifier ?What are the various types of amplifiers (3M)

PART -B

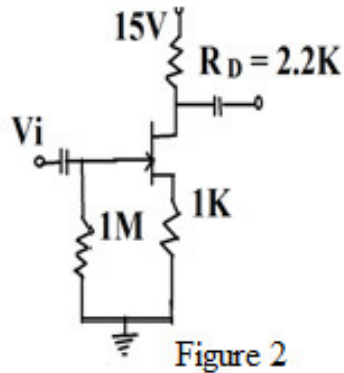
2. a) Derive continuity equation and state its special cases (7M)
- b) The mobility of free electrons and holes in pure silicon are 0.13 and $0.05m^2/V - s$ and the corresponding values for pure germanium are 0.38 and $0.18m^2/V - s$ respectively .Determine the values intrinsic conductivity for both silicon and germanium. Given that $n_i = 2.5 \times 10^{19}/m^3$ for geranium and $n_i = 2.5 \times 10^{19}/m^3$ for silicon at room temperature. (7M)
3. a) Derive the expression for diffusion capacitance in PN junction (7M)
- b) Explain in detail about V-I characteristics of a zener diode. (7M)
4. a) Draw and explain the circuit diagram of full wave rectifier with inductor filter (7M)
- b) A zener diode shunt regulator circuit is to be designed to maintain a constant load current $400mA$ and voltage $40V$. The input voltage is $90 \pm 5V$. The zener voltage is $40V$ and its dynamic resistance is 2.5Ω . Find the following quantities for regulator: (a) the series dropping resistance (b) zener power dissipation (c) load resistance .assume the zener current to be 10% of load current. (7M)
5. a) Explain input and output characteristics of a transistor in CE configuration (7M)
- b) Explain the four distinct regions of the output characteristics of JFET (7M)
6. a) What is thermal runaway? Explain how it can be avoided. (6M)
- b) A silicon transistor with $\beta=80$ is use in self-biasing arrangement with $V_{CC} = 15V$, $R_C = 4.7k\Omega$. The operating point Q is at $V_{CE} = 8.2V$, $I_C = 1.2mA$. find values R_1 , R_2 and R_E . (8M)

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SET - 2

7. a) For a common source amplifier as shown in Figure 2, operating point is defined by $V_{GSQ} = -2.5V$, $V_P = -6V$ & $I_{DQ} = 2.5mA$ with $I_{DSS} = 8mA$. Calculate g_m , r_d , Z_i , Z_o & Voltage gain A_v (7M)



- b) Derive the expressions for Z_i , Z_o and A_v for common drain J-FET amplifier (7M)

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2. Answer **ALL** the question in **Part-A**

3. Answer any **FOUR** Questions from **Part-B**

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**PART -A**

1. a) What is diffusion current? (2M)
- b) Write the Application of PN junction diode (2M)
- c) What is need for filters in power supplies? (2M)
- d) Compare JFET with BJT (3M)
- e) What is need for biasing a transistor? (2M)
- f) What is h-parameter for a transistor? (3M)

**PART -B**

2. a) Prove that Fermi level lies in the Centre of forbidden band for intrinsic semiconductor (7M)
- b) The resistivity of pure silicon is  $2.3 \times 10^6 \Omega \cdot \text{cm}$  at  $27^\circ\text{C}$ . Calculate intrinsic concentration at  $127^\circ\text{C}$  (7M)
3. a) Derive the expression for Transition capacitance in PN junction (7M)
- b) Explain the tunneling effect with the help neat diagrams (7M)
4. a) Derive expression for ripple factor and rms value of voltage of full wave rectifier with resistive load (7M)
- b) An L-C filter is to be used to provide a dc output with 1% ripple filter from a full-wave rectifier operating at 50Hz. Assume  $L/C = 0.01$ , determine the required values of L and C (7M)
5. a) Calculate the collector current and emitter current for a transistor with  $\alpha_{dc} = 0.99$  and  $I_{CBO} = 50\mu\text{A}$  when the base current is  $20\mu\text{A}$  (7M)
- b) Explain construction of n channel JFET with neat diagram (7M)
6. a) determine the stability factor for a CB amplifier circuit (7M)
- b) In voltage divider bias circuit, if  $V_{CC} = 10\text{V}$ ,  $V_{CE} = 5\text{V}$ ,  $I_C = 1.2\text{mA}$ ,  $R_2 = 10\text{k}\Omega$ ,  $\beta = 100$  and  $R_E = 270\Omega$ , calculate  $R_1$  and  $R_3$ . assume  $V_{BE(\text{act})} = 0.6\text{V}$  (7M)
7. a) Draw the hybrid parameter equivalent circuit for an NPN common emitter transistor and explain. (7M)
- b) For common source amplifier  $V_{GSQ} = -2\text{V}$ ,  $I_{DSS} = 8\text{mA}$ ,  $V_p = -8\text{V}$ ,  $Y_{os} = 20\mu\text{S}$ ,  $R_G = 1\text{M}\Omega$ ,  $R_D = 5.1\text{k}\Omega$ , calculate  $g_m$ ,  $r_d$ ,  $Z_i$ ,  $Z_o$  and  $A_v$  (7M)

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**SET - 4**
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 2. Answer **ALL** the question in **Part-A**

 3. Answer any **FOUR** Questions from **Part-B**

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PART -A

1. a) What is drift current? (2M)
- b) Define the term transition capacitance C_T of PN junction diode (3M)
- c) What are the advantages of bridge rectifier? (3M)
- d) What is early effect? (2M)
- e) What is meant by Q-point? (2M)
- f) Write the advantages of h-parameters. (2M)

PART -B

2. a) Derive the expression for the conductivity of extrinsic n type and p type semiconductor. (7M)
- b) Calculate the resistivity of silicon if donor type of impurity is added to the extent of 1 atom per 10^8 silicon atom, at $300^\circ K$ and assume $\mu_n = 1300 \text{ cm}^2/\text{V-s}$ (7M)
3. a) Derive the expression for Dynamic Resistor in PN junction (7M)
- b) Explain the working principle of PIN diode (7M)
4. a) Derive expression for ripple factor in full wave rectifier using inductor filter (7M)
- b) Design a zener regulator for following specification: load current=20mA, output voltage=5V, zener wattage=500mW, input voltage= $12 \pm 2\text{V}$ and $I_{Z\min}=8\text{mA}$. (7M)
5. a) A transistor operating in CB configuration has $I_C = 2.98\text{mA}$ and $I_E = 3\text{mA}$ and $I_{CO} = 0.01\text{mA}$ what current will flow in collector circuit, of this transistor when connected in CE configuration with a base current of $30\mu\text{A}$ (7M)
- b) Draw and explain the drain characteristics of n-channel enhancement type (7M)
6. a) Derive the expression for stability factor of a collector to base bias circuit (7M)
- b) Determine the operating point for the circuit of a potential divider bias arrangement with $R_2 = R_C = k\Omega$, $R_E = 1k\Omega$ and $R_1 = 40k\Omega$ (7M)
7. a) Explain in detail about the h-parameters using a two port network model (7M)
- b) The amplifier utilizes n-channel FET using source self bias circuit for which $V_p = -2\text{V}$, $I_{DSS} = 1.65\text{mA}$. It is desired to bias the circuit at $I_D = 0.8\text{mA}$, $A_v = 20\text{dB}$ using $V_{DD} = 4\text{V}$. Assume $r_d \gg R_D$, find i) V_G ii) g_m iii) R_s iv) R_D (7M)