Code No: RT31026 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2017

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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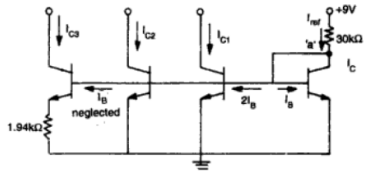
PART –A

1	a)	Discuss the role of a level translator in op amp.	[4M]
	b)	Discuss the features of voltage regulator.	[3M]
	c)	Design a adder circuit using an op amp to get output expression V_0= -(0.1 V_1+V_2+10V_3)	[4M]
	d)	Explain the principle of VCO.	[4M]
	e)	What are the advantages and disadvantages of active filter over passive?	[4M]
	f)	Define the terms: Linearity, settling time with respect to DAC.	[3M]

PART -B

2	a)	Explain the cascade differential amplifier stages.	[4M]
	b)	For the circuit shown below fig .Find the I_{C1}, I_{C2} and I_{C3}. Assume β=125.	[8M]



	c)	Compare the different configurations of differential amplifier.	[4M]
3	a)	Discuss the causes and equation for slew rate.	[4M]
	b)	Design an offset compensating network for a given op amp to meet the specified requirements.	[8M]
	c)	Discuss about the 78xx series regulator.	[4M]
4	a)	Draw an AC voltage follower and explain.	[4M]
	b)	What is a comparator? Discuss the non inverting comparator and obtain its input and output waveforms.	[8M]
	c)	Discuss the application of op amp as a current to voltage converter.	[4M]
5	a)	Discuss the 555 timer in monostable operation. Also discuss the applications for it.	[10M]
	b)	Explain how the PLL can be used as a FSK demodulator?	[6M]
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6	a)	Draw a second order filter and obtain the frequency response and output voltage for it.	[8M]
	b)	Design a WBPF having fl=400Hz, fh=2KHz with a pass band gain of 4. Find Q of the filter.	[8M]
7	a)	Draw the functional diagram of a dual slope integrating type ADC and also obtain expression for the output voltage.	[8M]
	b)	What are the important observations can be made for dual slope integrating type ADC and draw backs of it.	[5M]
	c)	What would be the output voltage produced by a D/A converter whose output range is 0 to 10V with a binary number s 10111100(for a 8 bit DAC)	[3M]

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