Code No: RT31026 **R13** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, October/November -2017

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	What is active load? Where it is used and Why?	[4M]
	b)	A square wave of peak to peak amplitude of 500 mv has to be amplified to a peak-to-peak amplitude of 3 V, with a rise time of 4 µSec. or less. Can a 741 be used?	[4M]
	c)	Draw the logarithmic amplifier circuit	[3M]
	d)	Draw the typical connection diagram of VCO 566 and what are its features	[4M]
	e)	Draw the active notch filter and what are its features	[4M]
	f)	What is the need for A/D and D/A conversion?	[3M]

PART -B

2	a)	Present the a.c analysis of differential amplifier using h-parameters. Find A_d,A_c,R_i and R_o for dual input balanced output configuration.	[8M]
	b)	For a dual input unbalanced output differential amplifier, various circuit parameters are $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 10V$, R_C=4.7KΩ, R_E=6.8KΩ, R_{S1}=R_{S2}=50Ω, β_{dc}=β_{ac}=49 and V_{BE}=0.7V. Find Q-Point, Voltage gain, Input Resistance, Output Resistance.	[8M]
3	a)	Explain the process of measuring open loop voltage gain and input bias current in op-amp	[8M]
	b)	Draw and explain the working of Bias current compensations circuit.	[8M]
4	a)	Draw and explain the non-inverting summing amplifier.	[8M]
	b)	Design the op-amp circuit which can give the output as V_O=$2V_1$-$3V_2$+$4V_3$-$5V_4$.	[8M]
5	a)	Derive expression for the duty cycle of Astable multivibrator using IC 555 with a neat circuit and waveforms.	[8M]
	b)	Design a square wave generator of frequency 100 Hz and duty cycle of 75%.	[8M]
6	a)	Design a second order Butterworth 50 Hz notch filter for removing line noise from an ECG signal.	[8M]
	b)	Design a wide band reject filter having f_H=200 Hz and f_L= 2 KHz, assume suitable data.	[8M]
7	a)	Explain the operation of multiplying DAC and mention its applications.	[8M]
	b)	The logic levels used in an 8-bit R-2R ladder type DAC ARE LOGIC '1' = +5 volts and logic '0' = 0 volts. Find the output voltage for an input of 10110111.	[8M]

*****
~~~~~~

Code No: RT31026 **R13** SET - 2

III B. Tech I Semester Regular/Supplementary Examinations, October/November -2017

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1 a) The common mode input to a differential amplifier with a differential gain of 120 is 2 Sin 100πt V. find the common mode output if CMRR is 60 dB. [4M]
b) What are the characteristics of IC Voltage regulators? [4M]
c) Draw the instrumentation amplifier. [3M]
d) Draw the Schmitt trigger circuit using IC 555. [4M]
e) Draw the frequency response characteristics of high pass filter. [3M]
f) State the advantages and applications of sample and hold circuits. [4M]

PART -B

2 a) Determine the voltage gain of FET based differential amplifier with active load. [8M]
b) Design the dual input and balanced output differential amplifier using diode the constant current bias to meet the following specifications and draw the designed circuit. [8M]
i) Supply voltage = ±10V
ii) Emitter current I_E in each differential amplifier transistor is 1.5 mA and V_{BE}=0.7 V
iii) Voltage gain ≤ 60

3 a) Explain the process of measuring input offset voltage and PSRR in op-amp. [8M]
b) Draw and explain the working of Output offset voltage balancing circuit. [8M]

4 a) Draw the op-amp based subtractor circuit and show that the output is proportional to the difference of the two input voltages. [8M]
b) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to 1 kHz. If a sine wave of 1 V peak at 1000 Hz is applied to this differentiator, draw the output waveform. [8M]

5 a) Derive expression for the pulse width of Mono stable multi vibrator using IC 555 with a neat circuit and waveforms. [8M]
b) Design an Astable multi vibrator which will flash the electric bulb such that its ON time will be 3 seconds and off time will be 1 second. [8M]

6 a) Design a notch filter for f_N=8 kHz and Q = 10, Choose C = 500 pF [8M]
b) Design a first order wide band reject filter with a higher cutoff frequency of 100 Hz and a lower cutoff frequency of 1 KHz. Calculate the Q-factor of the filter. [8M]

7 a) Design a 4-bit weighted resistor DAC whose full scale output voltage is -10 volts. Assume R_f = 10 K, logic '1' level as +5 volts and logic '0' level as 0 volts. What is the output voltage when the input is 1011. [8M]
b) Discuss the R-2R ladder used in digital to analog conversion using suitable mathematical expressions. [8M]

*****
~~~~~~

Code No: RT31026 **R13** SET - 3

III B. Tech I Semester Regular/Supplementary Examinations, October/November -2017

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	Draw the emitter coupled differential amplifier	[4M]
	b)	Draw the circuit of a voltage regulator and explain	[4M]
	c)	Give the applications of instrumentation amplifier	[4M]
	d)	Draw the Astable multivibrator using IC 555	[3M]
	e)	Draw the frequency response characteristics of band elimination filter	[3M]
	f)	Find the step size and analog output when input is 1000 and 1111. Assume V_{ref} = 5 V	[4M]

PART -B

2	a)	Present the a.c analysis of differential amplifier using r-parameters. Find A_d,A_c,R_i and R_o for dual input balanced output configuration.	[8M]
	b)	Draw a circuit in which the output current is forced to equal the input current.	[8M]
3	a)	Discuss the measurement of CMRR and output offset voltage in op-amp	[8M]
	b)	Draw the schematic diagram and explain about Dual power supply using 78XX and 79XX integrated circuits.	[8M]
4	a)	Draw the three op-amp instrumentation amplifier and derive expression for its overall gain.	[8M]
	b)	Draw the active integrator circuit and discuss about its frequency response.	[8M]
5	a)	Derive expression for the voltage to frequency conversion factor of a VCO.	[8M]
	b)	With the help of a block diagram determine the capture range of PLL.	[8M]
6	a)	Design a notch filter for f_N = 8 KHz and Q = 10, choose C = 500 pF.	[8M]
	b)	Design a second order Butterworth 50 Hz notch filter for removing line noise from an ECG Signal.	[8M]
7	a)	Calculate the conversion time for a full scale input in case of a 12-bit counter type ADC driven by 4 MHz clock	[6M]
	b)	Draw the block diagram and illustrate the conversion process of the successive approximation A/D Converter	[10M]

*****
~~~~~~

Code No: RT31026 **R13** SET- 4

III B. Tech I Semester Regular/Supplementary Examinations, October/November -2017

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	Draw the current mirror circuit? What are its advantages?	[4M]
	b)	Derive expression for slew rate of an op-amp.	[4M]
	c)	Draw the voltage to current converter circuit using op-amp.	[3M]
	d)	Draw the Monostable multivibrator using IC 555.	[4M]
	e)	What are the advantages of active filters.	[3M]
	f)	State the advantages of tracking converter over the counter type converter.	[4M]

PART -B

2	a)	How the active loads are used to improve CMRR of a differential amplifier? Explain with a neat circuit	[8M]
	b)	Draw the circuit and explain about the cascaded differential amplifier.	[8M]
3	a)	Discuss the measurement of output resistance and CMRR in op-amp.	[8M]
	b)	Draw and explain the working of Output offset voltage balancing circuit.	[8M]
4	a)	Draw the active differentiator and give the complete frequency response of it.	[8M]
	b)	Design a differentiator that will differentiate an input signal with f_{max}=100 Hz.	[8M]
5	a)	Draw the transfer characteristics of PLL and present its closed loop analysis.	[8M]
	b)	With the help of a block diagram determine the lock range of PLL.	[8M]
6	a)	Design and obtain the frequency response of a band pass filter with f_L = 500 Hz and f_H = 2 kHz with pass band gain 1.	[8M]
	b)	Design a wideband reject filter having f_H = 500 Hz and f_L = 3 KHz with a pass band gain of 2.	[8M]
7	a)	Discuss in detail about the dual slope ADC	[8M]
	b)	Draw the inverted R/2R ladder D/A Converter in current steering mode and derive for the output voltage.	[8M]

*****
~~~~~~