Code No: RT22023 **R13** SET - 1

II B. Tech II Semester Regular/Supplementary Examinations, April/May-2017
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Write the application of attenuator (4M)
   b) State the clamping theorem (3M)
   c) Write the application of Monostable multi vibrator (3M)
   d) Draw the diagram for Diode two input AND gate (4M)
   e) Define the terms i) voltage time base generator ii) current time base generator (4M)
   f) What are the advantages and disadvantages of unidirectional diode gate (4M)

PART –B

2. a) Derive an expression for the upper cut-off frequency of low pass RC circuit (8M)
   b) A symmetrical square wave whose peak-to-peak amplitude is 2V and whose average value is zero as applied to on RC integrating circuit. The time constant is equals to half -period of the square wave? find the peak to peak value of the output amplitude (8M)

3. a) Explain how a sine wave may be converted into a square wave using a clipping circuit (8M)
   b) T=1000 μ sec (8M)
   V= 10 V
   Duty cycle = 0.2
   i) Sketch waveform with voltage levels at steady state Figure 1.
   ii) Forward and reverse direction tilt
   iii) Af/ Ar

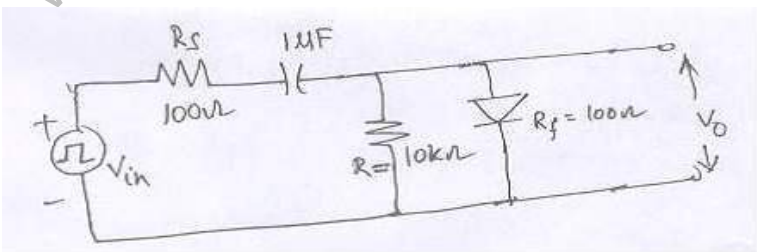

Figure 1
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4. a) Derive an expression for the gate width of a mono-stable multivibrator (8M)
   b) A collector coupled Fixed bias binary uses NPN transistors with h_{FE}= 100. The circuit parameters are VCC = 12v, VBB = -3v, RC = 1k , R1 = 5k , and R2 = 10 k. Verify that when one transistor is cut-off the other is in saturation. Find the stable state currents and voltages for the circuit. Assume for transistors VCE(sat) = 0.3V and VBE(sat) = 0.7V (8M)

5. a) What is positive and negative logic system (8M)
   b) With the help of a neat circuit diagram for NOR gate using ECL logic and explain. (8M)

6. a) Explain with neat diagram and working of a UJT time base generator (8M)
   b) Explain the basic principles of the Miller and bootstrap time base generator (8M)

7. a) How does the synch signal affect the frequency of operation of the sweep generator? (8M)
   b) Explain use of a mono stable relaxation device as a divider (8M)

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PART –A

1. a) What do you mean by (i) over compensation (ii) under compensation (4M)
   b) What is the difference between clipping and clamping (4M)
   c) What are the applications of Schmitt trigger? (3M)
   d) Draw the diagram for Diode two input OR gate (4M)
   e) Draw the sweep waveform and define the parts of the waveform? (4M)
   f) What are the advantages with diode sampling gate (3M)

PART -B

2. a) Derive an expression for the rise time of the output of a low pass circuit excited by a step input (8M)
   b) Three low pass RC circuits are in cascade and isolated from one another by ideal buffer amplifiers. Find the expression for the output voltage as a function of time if the input is a step voltage. (8M)

3. a) With the help of a neat circuit diagram, explain the working of an emitter-coupled clipper (8M)
   b) The input voltage vi to the two level clipper shown in Figure 1, varies linearly from 0 to 75 V. Sketch the output voltage vo to the same time scale as the input voltage. Assume Ideal diodes. (8M)

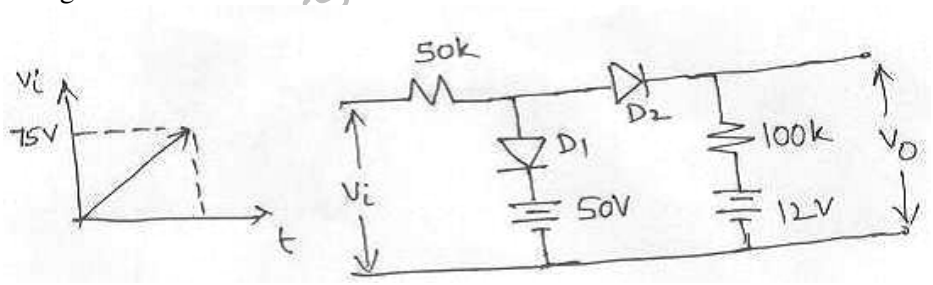

Figure 1

4. a) Derive an expression for the UTP and LTP of Schmitt trigger. (8M)
   b) Design a collector coupled transistor monostable multivibrator to produce a time delay of 100 μ sec. Use transistors have h_{FE} of 250. Use ±12 v sources, $V_{CE}(sat)$ = 0.3 v, $V_{BE}(sat)$ = 0.7 v and V_{BE} cutoff = 0v. (8M)
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5. a) Explain with suitable diagram of 3-input AND gate TTL? (8M)
   b) With the help of a neat circuit diagram for NAND gate using ECL logic and explain. (8M)

6. a) Define below terms and derive the relation between (8M)
      i) sweep speed error
      ii) displacement error
      iii) transmission error
   b) Explain in detail the working of a transistor Miller time-base generator (8M)

7. a) Explain in detail frequency division by an astable blocking oscillator (8M)
   b) Explain the synchronization of a sweep circuit with symmetrical signals (8M)

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) If IV is the peak to peak of differentiator? What is the output of peak to peak? (4M)
   b) What is shunt noise clipper (3M)
   c) What is a non-saturated binary? Write its advantages and disadvantages (3M)
   d) Write the advantages and disadvantages of TTL family (4M)
   e) Define flyback time and sweep time? (4M)
   f) What are the drawbacks of two diode gates? (4M)

PART -B

2. a) Derive an expression for the output of a high-pass circuit excited by a ramp input (8M)
   b) Sketch the output waveform for square wave input. A pulse of 5 v amplitude and pulse width 0.5 m sec is applied to high pass RC circuit consisting of R = 22 kΩ and C = 0.47 μf. Determine the % tilt in the output waveform. (8M)

3. a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the Figure 1. (8M)

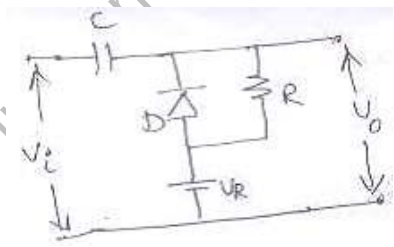

Figure 1

   b) Compare and explain series diode clipper and shunt diode clipper. (8M)

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a Astable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors. (16M)

5. a) Define positive and negative logic system (8M)
   b) With the help of a neat circuit diagram for NAND gate using NMOS logic and explain. (8M)

6. a) Explain various methods of generating time- base waveforms (8M)
   b) Explain general considerations of bootstrap time base generator (8M)

7. a) Explain synchronization of a sweep generator with pulse signals (8M)
   b) Explain use of a mono stable relaxation device as a divider (8M)
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Code No: RT22023 **R13** SET - 4

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Draw the circuit of double differentiator (4M)
   b) What is series noise clipper (3M)
   c) Write the difference between saturated and non-saturated binary (4M)
   d) Write the advantages and disadvantages of DTL family (4M)
   e) What are the applications of time base generator (3M)
   f) What is basic operating principles of sampling gates (4M)

PART –B

2. a) Derive the condition for perfect compensator of an attenuator (8M)
   b) Derive the expression for percentage till for a square wave output of RC high pass circuit. (8M)

3. a) State and prove the clamping circuit theorem (8M)
   b) Determine Vo for the network shown in Figure 1, for the given waveform Assume ideal diodes. (8M)

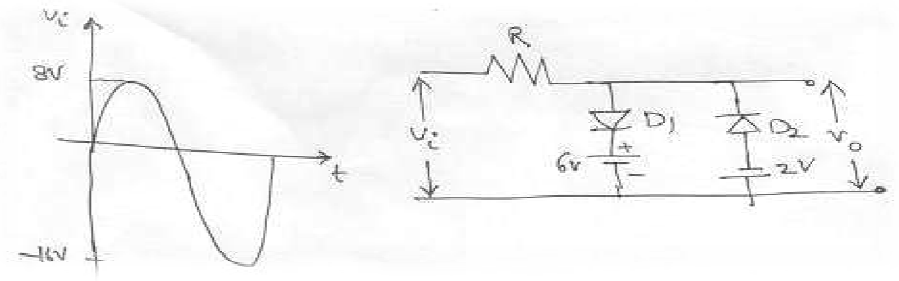

Figure 1

4. With neat diagram explain how to control hysteresis in Schmitt trigger? (16M)

5. a) Explain in detail about CMOS logic-analysis (8M)
   b) With the help of a neat circuit diagram for NAND gate using PMOS logic and explain. (8M)

6. a) Explain in detail about transistor constant current sweep (8M)
   b) Explain the effect of gate width w.r. to voltage in boot strap circuit (8M)

7. a) What is the condition to met for pulse synchronization of mono-stable circuits (8M)
   b) With the help of neat waveforms, explain sine wave frequency division with a sweep circuit (8M)
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