

Code No: **R42046**

R10

Set No. 1

IV B.Tech II Semester Supplementary Examinations, April/May - 2017

STRUCTURED DIGITAL DESIGN

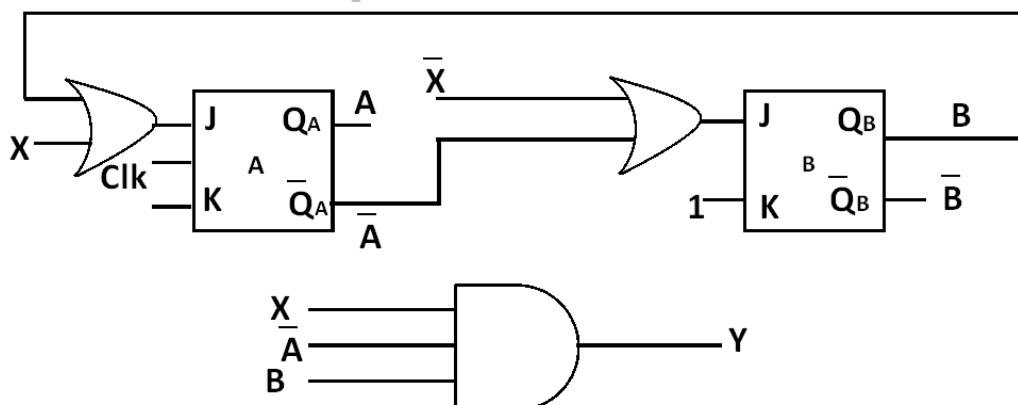
(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time: 3 hours

Max. Marks: 75

Answer any FIVE Questions
All Questions carry equal marks

- 1 a) Explain the Top down digital design methodology. [7]
b) Explain about data objects in VHDL [4]
c) Discuss the binding? Discuss the binding between entity and components. [4]
- 2 a) Explain the structure of various LOOP statements in VHDL with examples. [5]
Explain the syntax and structure of a package and configurations in VHDL. [5]
b) What is meant by logic synthesis? How is it useful in the design of digital circuits [5]
- 3 a) Draw the structure of a 8-bit counter. Write the VHDL description for the same. [8]
b) Explain about signal assignment statements and Variable assignment statements with example. [7]
- 4 a) Write the behavioral description for JK FF with active low preset and clear inputs. [7]
b) Derive the state equation, state table and state diagram for the sequential circuit shown below



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- 5 a) Design and implement a full adder using Verilog HDL.
i) gate level modeling ii) Structural modeling (using half adder) [7]
b) Write the verilog code for a 2:4 decoder circuit. [4]
c) Explain in detail net, gate and tri-state delays with examples and Verilog code? [4]
- 6 a) Draw the basic functional unit of a dynamic shift register using switch level modelling. and write a Verilog module with test bench. [8]
b) Briefly explain combinational and sequential UDPs in Verilog. Also write Verilog module for D latch using UDP.. [7]
- 7 a) Design a counter module and test bench to illustrate the use of WAIT construct in a Verilog. [8]
b) Explain the Synthesis of sequential logic. How is it different compared to Combinational synthesis. [7]
- 8 a) Explain stuck at 0 and stuck at 1 faults in logic circuits [8]
b) Explain the test pattern generation in BIST circuits. [7]