Code No: R22023 **R10** SET - 1

II B. Tech II Semester Supplementary Examinations, April/May-2017
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Subtract 27810 from 49510 using the excess-3 subtractor. (5M)
   b) Encode the decimal number using 6, 3, 1,-1 weighted code. Is it a self complementing code? (5M)
   c) Write first 20 numbers in radix-6 (5M)

2. a) The message below has been coded in Hamming code. Decode the message for single error detection code (message = 4 bits).1001001 0111001 1110110 0011011. (8M)
   b) Realize an 2 input EX-OR gate using minimum number of 2 input NAND gates. (7M)

3. a) Difference between K map and Tubular method (5M)
   b) Minimize the given 5 variable function using QM Tabular Method (10M)
   $f = \Sigma (2, 4, 9, 10, 11, 12, 19, 20, 21, 22, 23, 24, 25, 26, 29, 31)$.

4. a) Design4 bit adder-subtractor circuit and explain in detail. (8M)
   b) Explain about look-a-head adder circuit. (7M)

5. a) Design a 5 to 32 line decoder using 3 to 8 line decode, active low outputs with 2 active low and one active high enable (8M)
   b) Implement $f(A,B,C,D) = \Sigma (0,1,3,5,6,8,9,11,12,13)$ using 8:1 MUX (7M)

6. a) Write the difference between PLA, PAL. (5M)
   b) Implement $f(A,B,C,D) = \sum(0,1,4,5,6,7,9,10,12,13,15)$ using PAL and explain its procedure (10M)

7. a) What is a master slave flip flop? Design a clocked master slave JK flip flop. (8M)
   b) Design a synchronous modulo-12 counter using NAND gates and JK flip flops. (7M)

8. a) Write the difference between moor and mealy machine (4M)
   b) Reduce the number of states in the following state table and tabulate the reduced state table (11M)

PS	NS_1Z	
	x=0	*x=1*
A	D, 0	H, 1
B	F, 1	C, 1
C	D, 0	F, 1
D	C, 0	E, 1
E	C, 1	D, 1
F	D, 1	D, 1
G	D, 1	C, 1
H	B, 1	A, 1
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