Code No: R1621042 **R16** SET - 1

II B. Tech I Semester Model Question Paper Oct/Nov - 2017
SWITCHING THEORY AND LOGIC DESIGN
(Com. to ECE, ECC, EIE.)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A [7 x 2 =14]

1. a) Write the differences between combinational and sequential circuits.
   b) State De Morgans's theorems
   c) List the applications of Multiplexers.
   d) Write the demerits of PROM
   e) Write the differences between combinational and sequential circuits.
   f) Sketch Mealy circuit and explain.
   g) What is race around condition? How can minimized in J-K flip-flop

PART –B

2. a) Given the 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors (10M)
   b) Perform the following addition using excess-3 code i)386+756 ii)1010 + 444 (4M)

3. Simplify the following using tabulation method (14M)
   $y(w,x,y,z)=\sum m(1,2,3,5,9,12,14,15)+d(4,8,11)$

4. a) Design a excess-3 adder using 4-bit parallel binary adder and logic gates. (10M)
   b) What are the applications of full adders? (4M)

5. a) Design and implement Full adder with PLA (7M)
   b) Write the comparisons between PAL, PLA (7M)

6. a) Construct a JK flip flop using a D flip flop, a 2x1 multiplexer and an inverter. (7M)
   b) Draw the schematic circuit of RS master slave flip flop. Give its truth table and justify the entries in the truth table. (7M)

7. a) Draw the diagram of Mealy type FSM for serial adder. (7M)
   b) Draw the circuit for Moore type FSM. (7M)

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PART –A

[7 x 2 =14]

1. a) Perform $(24)_{10} - (56)_{10}$ in BCD using 9's complement
   b) State De Morgans's theorems.
   c) Design 2x4 decoder using NAND gates.
   d) Give the comparison between PROM, PLA and PAL.
   e) What are applications of Flip-Flop?
   f) Write capabilities and limitations of Finite- State machine.
   g) Implement two input EX-OR gate from 2 to 1 multiplexer

PART –B

2. a) Convert the given expression in standard SOP form f(A,B,C)=AC+BA+BC (7M)
   b) Convert the given expression in standard POS form y=A.(A+B+C) (7M)

3. a) Reduce the following function using k-map technique F(A,B,C,D)=π(0,2,3,8,9,12,13,15) (7M)
   b) Minimize the expression using k-map y=(A+B+C') (A+ B+ C) (A' + B' + C') (A' + B +C) (A+B+C) (7M)

4. a) Design BCD to gray code converter and realize using logic gates. (7M)
   b) Design a 1:8 demultiplexer using two 1:4 demultiplexer. (7M)

5. a) Implement the following Boolean functions using PLA. A(x,y,z)=∑(1,2,4,6) B(x,y,z)= ∑(0,1,6,7) C(x,y,z)= ∑(2,6) (7M)
   b) Design a combinational circuit using PROM that accepts 3-bit binary number and generates its equivalent excess-3 code. (7M)

6. a) Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table. (7M)
   b) Convert D flip-flop into T and JK flip-flops. (7M)

7. a) The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x2 changes from 0 to 1 while x1=1. The output changes from 1 to 0 only when x1 changes from 1 to 0 while x2=1. Find a minimum row reduced flow table (7M)
   b) Draw a state diagrams of a sequence detector which can detect 101 (7M)

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Code No: R1621042 **R16** SET - 3

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PART –A

[7 x 2 =14]

1. a) Convert $(97.75)_{10}$ to base 2.
   b) Prove that OR-AND network is equivalent to NOR-NOR network.
   c) Realize full adder using two half adders and logic gates.
   d) Design a 4x2 PROM with AND-OR gates.
   e) Distinguish between Moore and Mealy Machines.
   f) Write and prove de-Morgan laws
   g) Draw the diagram of subtractor using truth tables.

PART -B

2. Find the complement of the following Boolean functions and reduce them to minimum number of literals. (7M)
   a) (b c' +a' d) (ab' +cd') (7M)
   b) (b' d+ a' b c' +a c d+ a' b c) (8M+8M)

3. Simplify the following Boolean expressions using K-map and implement it by using NOR gates. a) F(A,B,C,D)=AB'C' +AC+A'CD' (7M)
   b)F(W,X,Y,Z)=w' x'y'z' + wxy'z' + w'x'yz + wxyz

4. a) Design and implement a two bit comparator using logic gates. (7M)
   b) Implement full adder using decoder and OR gates. (7M)

5. a) Design a BCD to excess-3 code converter and implement using suitable PLA. (7M)
   b) Implement the following functions using a PROM i) F(w,x,y,z)=∑(1,9,12,15) (7M)
   ii) G(w,x,y,z)= ∑(0,1,2,3,4,5,7,8,10,11,12,13,14,15)

6. a) Draw the logic diagram of a JK flip- flop and using excitation table explain its operation. (7M)
   b) What do you mean by triggering? Explain the various triggering modes with examples. (7M)

7. a) Explain about sequential circuits, state table and state diagram. (7M)
   b) Explain the procedure of Meelay to Moore conversion. (7M)

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PART –A [7 x 2 =14]

1. a) Convert$(2468)_{10}$ to $(\ )_{16}$
   b) What are the advantages of tabulation method over K-map?
   c) Why a multiplexer is called a data selector? Draw the 2x1 MUX.
   d) Write a brief note on PLDs
   e) Give the comparison between synchronous sequential and asynchronous sequential circuits
   f) Draw and explain Moore circuit.
   g) Draw the basic architecture of a PAL?

PART -B

2. a) What is the difference between canonical form and standard form? Explain (7M)
   b) How are negative numbers represented? Represent signed numbers from +7 to -8 (7M)

3. a) Simplify the following using K- map and implement the same using NAND gates. (7M)
   Y (A, B, C) =∑(0,2,4,5,6,7)
   b) R Represent and draw the following Boolean function using minimum number of basic gates. i) (AB + AB') (AB)' ii) [(ABD(C + D + E)) + (A +DBC)'] (ABC + (CAD)') (7M)

4. a) Define decoder. Construct 3x8 decoder using logic gates and truth table. (7M)
   b) Define an encoder. Design octal to binary encoder. (7M)

5. a) Design and implement Full adder with PLA (7M)
   b) Design a combinational circuit using PROM. The circuit accepts a 3 bit number and generates an O/p binary number equal to square of input number. (7M)

6. a) Convert JK flip-flop to T flip-flop (7M)
   b) Convert RS flip-flop to D flip-flop (7M)

7. A clocked sequential circuit is provided with a single input x and single output z, whenever the input produces a string pulsed 111 or 000 and at the end of the sequence it produces an output z=1 and overlapping is also allowed. (7M)
   a) Obtain state diagram and state table. (7M)
   b) Find equivalence classes using partition method and design the circuit using D flip-flop.

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